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MICROCOMPUTER MN102L

MN102L610B/F61G
LSI User's Manual

Pub.No.22261-011E

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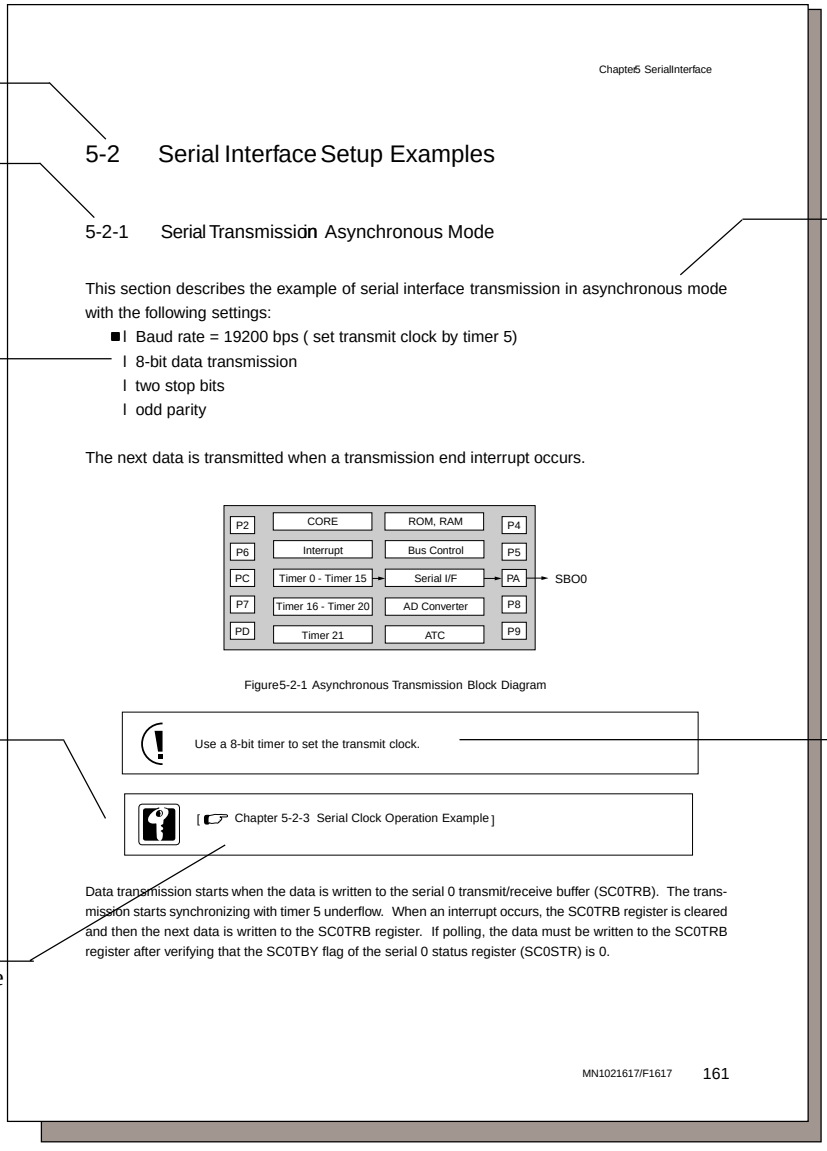
About This Manual

This manual is intended for assembly-language programming engineers. It describes the internal configuration and hardware functions of this microcontroller by block basis.

■Manual Configuration

Each section of this manual consists of a title, summary, main text, key information, precautions and warnings, and references.

The layout and definition of each section are shown below.


Chapter5 SerialInterface
5-2 Serial Interface Setup Examples
5-2-1 Serial Transmission in Asynchronous Mode
This section describes the example of serial interface transmission in asynchronous mode with the following settings:
■ Baud rate = 19200 bps (set transmit clock by timer 5)
■ 8-bit data transmission
■ two stop bits
■ odd parity
The next data is transmitted when a transmission end interrupt occurs.
P2
CORE
ROM, RAM
P4
P6
Interrupt
Bus Control
P5
PC
Timer 0 - Timer 15
Serial I/F
PA
SBO0
P7
Timer 16 - Timer 20
AD Converter
P8
PD
Timer 21
ATC
P9
Figure5-2-1 Asynchronous Transmission Block Diagram
Use a 8-bit timer to set the transmit clock.
[Chapter 5-2-3 Serial Clock Operation Example]
Data transmission starts when the data is written to the serial 0 transmit/receive buffer (SC0TRB). The transmission starts synchronizing with timer 5 underflow. When an interrupt occurs, the SC0TRB register is cleared and then the next data is written to the SC0TRB register. If polling, the data must be written to the SC0TRB register after verifying that the SC0TBY flag of the serial 0 status register (SC0STR) is 0.
MN1021617/F1617
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Subtitle

Sub-subtitle
The smallest block in this manual.

Main text

Summary
Introduction to the section.

Key information
Important information from the text.

Precautions and warnings
Precautions are listed in case.
Be sure to read these of lost functionality or damage.

References
References for the main text.

Finding Desired Information

This manual provides four methods for finding desired information quickly and easily.

(1) An index for the front of the manual for finding each section.

(2) A table of contents at the front of the manual for finding desired titles.

(3) A list of figures at the front of the manual for finding illustrations and charts by names.

(4) A chapter name is located at the upper corner of each page.

Related Manuals

- MN102L Series LSI User's Manual
  (Describes the MN102L series specifications)
- MN102L Series Instruction Manual
  (Describes the instruction set)
- MN10200 Series Liner Addressing Version C Compiler User Manual Usage Guide
  (Describes the installation, commands, and options for the C complier)
- MN10200 Series Liner Addressing Version C Compiler User Manual Language Description
  (Describes the syntax for the C complier)
- MN10200 Series Liner Addressing Version C Compiler User Manual Library Refer ence
  (Describes the standard libraries for the C complier)
- MN102L Series Cross Assembler User Manual Language Description
  (Describes the assembler syntax and notation)
- MN10200 Series Liner Addressing Version C Source Code Debugger User Manual
  (Describes the use of the C source code debugger)
- MN102L Series PanaXSeries Installation Manual
  (Describes the installation of the C complier, cross-assembler, and C source code debugger and the procedures for using the in-circuit emulator)

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Chapter 1 Overview

1

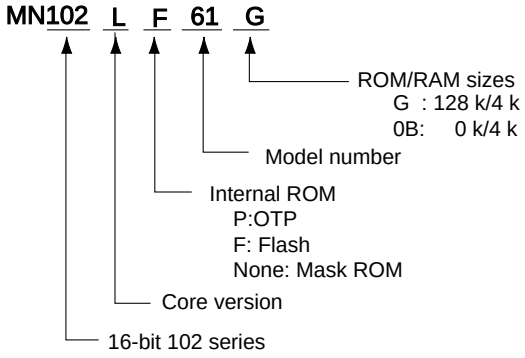
1-1 Overview

1-1-1 Introduction

The MN102 series linear addressing version designs the new architecture for C-language programming based on a detailed analysis for embedded applications. This improves the system architecture in speed and function to meet the requirements in user systems including miniaturization and low power consumption.

The MN102LF61G series contains sufficient peripheral equipments, four $\overline{CS}$ signals and a memory interface that supports burst ROM, and realize high-efficiency real-time control in variety of systems such as printer, electric musical instruments, audiovisual equipments, home electric appliances, cars, robots and computer peripherals.
The MN102L series adapts a load/store architecture method for computing within registers and a harvard architecture method for separating instructions bus and operand bus. Using one byte/one machine cycle basic instructions minimizes code size and improves compiler efficiency.

[Model Explanation]



1-1-2 Features

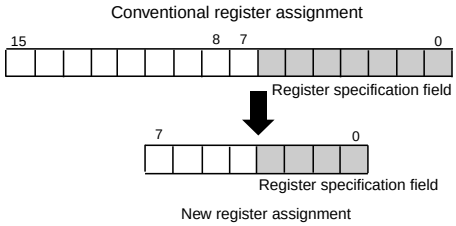
The MN102L series contains a flexible and optimized hardware architecture as well as a simple and efficient instruction set. It obtains economical efficiency and high speed.

1. Linear Addressing for Large Systems

The MN102L series contains up to 16 Mbytes of linear address space. The CPU provides an effective development environment without detecting borders between address spaces. The hardware architecture is also optimized for large systems. The memory is not divided into instruction space and data space so that operations can share instructions.

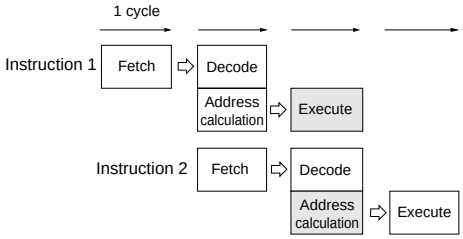
2. Single-byte Basic Instruction Length

The MN102L series has replaced general registers with eight internal CPU registers divided four address registers (A0 to A3) and four data registers (D0 to D3). The register specification fields are four bits or less, and the code sizes of the frequently used basic instructions including register- to-register operations and load/store operations are one byte.



3. High-speed Pipeline Processing

The MN102L series executes instructions in a 3-stage pipeline: fetch, decode and execute. This allows the MN102 series to execute instructions of single byte in one machine cycle (100 ns at 20 MHz).

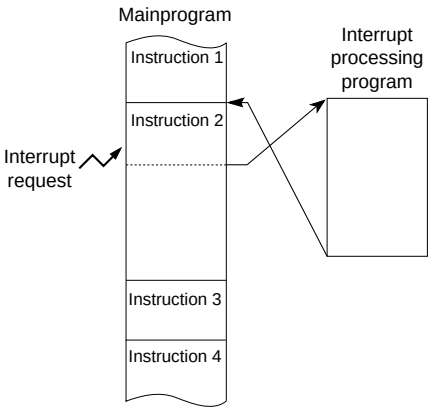


4. Simple Instruction Set

The MN102L series uses an instruction set of 36 instructions, designed specially for the programming model for embedded applications. To compress the code size, instructions have a variable length of one byte to five bytes. The most frequently used instructions in C-language compiler are single byte.

5. High-speed Interrupt Response

The MN102L series can respond quickly to interrupt handling even during the execution of the instruction with long execution cycles by suspending it. After an interrupt occurs, the program moves to the interrupt handler within 11 cycles or less. The MN102 series enhances real-time control performance using the interrupt handler which adjusts interrupt handling speed depending on user requirements.



6. Flexible Interrupt Control Structure

The interrupt controller is divided into eight groups (Group 0 is reserved for NMI.) and supports a maximum of four vectors for each group in total of 26 vectors. Each group can be set to one of seven priority levels. This provides the software design flexibility and accurate control. The CPU is compatible with software from previous Panasonic peripheral modules.

7. HIgh-speed, high-functionality external interface

The MN102L series provides DMA, handshaking, bus arbitration, and other functions that ensure a fast, efficient interface with other devices.

8. C-Language Development Environment

The MN102L series contains highly efficient C compiler and simple hardware optimized for C-language programming. With this advantage, this series improves development environment for C-language embedded applications without expanding the program size. The **PanaXSeries** development tools support the MN102 series devices.

9. Outstanding Power Savings

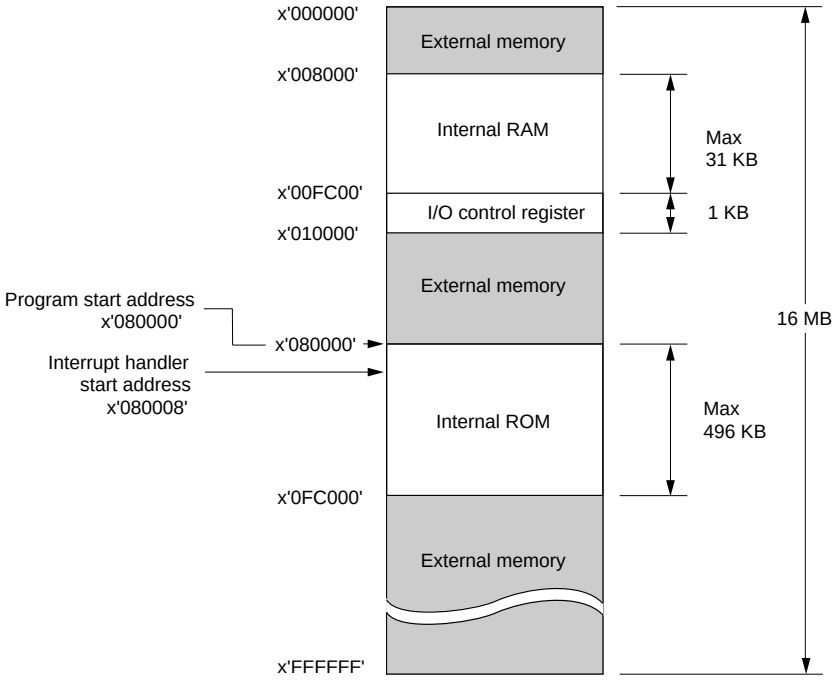
The MN102L series contains separate buses which distribute and reduce load capacitance. This greatly reduces overall power consumption compared to our conventional models. The MN102L series also supports three modes of SLOW, HALT and STOP for power savings.

1-1-3 Overview

This section describes the basic configuration and function of this series.

■ Address Space

The memory contains up to 16 MB linear address space. The instruction space and data space are not separated so that internal RAM and special function registers for internal peripheral functions are allocated into the first 64 KB in memory as the basic configuration. Table 1-1-1 shows three memory modes that supports each model and size of user program.



This is a general example of the memory expansion mode.

Both the start address and the end address of internal RAM are changed within x"008000" to x"00FBFF" depending on models.

The start address of internal ROM is fixed at x"080000" while the end address of internal ROM is changed depending on sizes of internal ROM. (The end address in this example is 496 KB.)

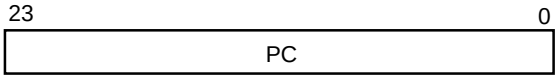
Figure 1-1-1 Address Space

Table 1-1-1 Memory Modes

Mode	Address bit width	Internal ROM capacity
Single chip mode	Up to 24 bits	16 KB or more
Memory expansion mode		
Processor mode		None

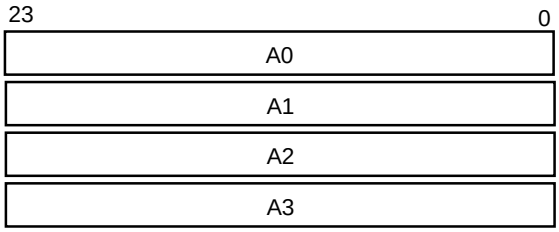
■ Internal Registers, Memory and Special Function Registers

Program Counter



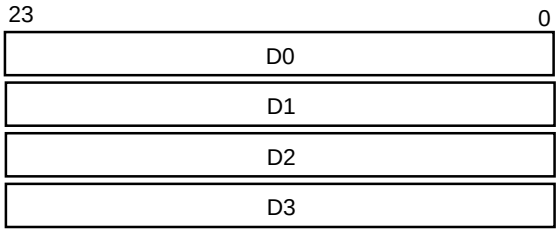
The program counter specifies the address (24 bits) of the program during the execution.

Address Registers



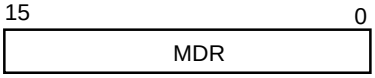
The address registers specify the data location on the memory. A3 is assigned as the stack pointer.

Data Registers



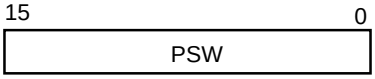
The data registers perform all arithmetic and logic operations. When the byte (8-bit) data or the word (16-bit) data is transferred to memory or another register, the instruction adds a zero or a sign extension.

Multiplication/Division Register



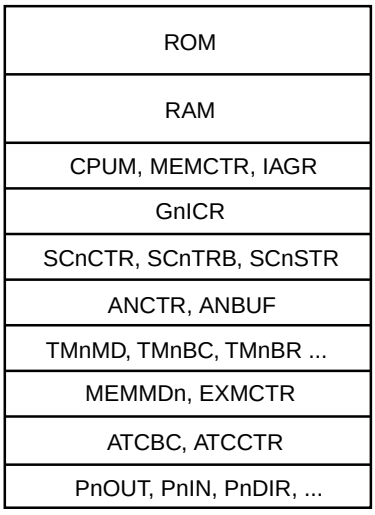
The multiplication/division register stores the upper 16 bits of the 32-bit product of the multiplication operations. In division operations, this register stores the upper 16 bits of the 32-bit dividend before the execution and the 16-bit remainder of the quotient after the execution.

Processor Status Word



The processor status word indicates the CPU status. This register stores the operation result flags and interrupt mask levels.

Memory, Special Registers, I/O Ports



Memory (ROM and RAM), special registers for controlling peripheral functions and I/O ports are assigned to the same address space.

Internal Control Registers

Interrupt Control Registers

Serial Interface

A/D Converter

Timers/Counters

Memory Control Registers

ATC Control Registers

I/O Ports

■ Interrupt Controller

The interrupt controller (group 0 to group 7) allocated to the outside of the CPU controls all nonmaskable interrupts and maskable interrupts except reset. Each group contains up to four interrupt vectors and specifies any of seven priority levels.

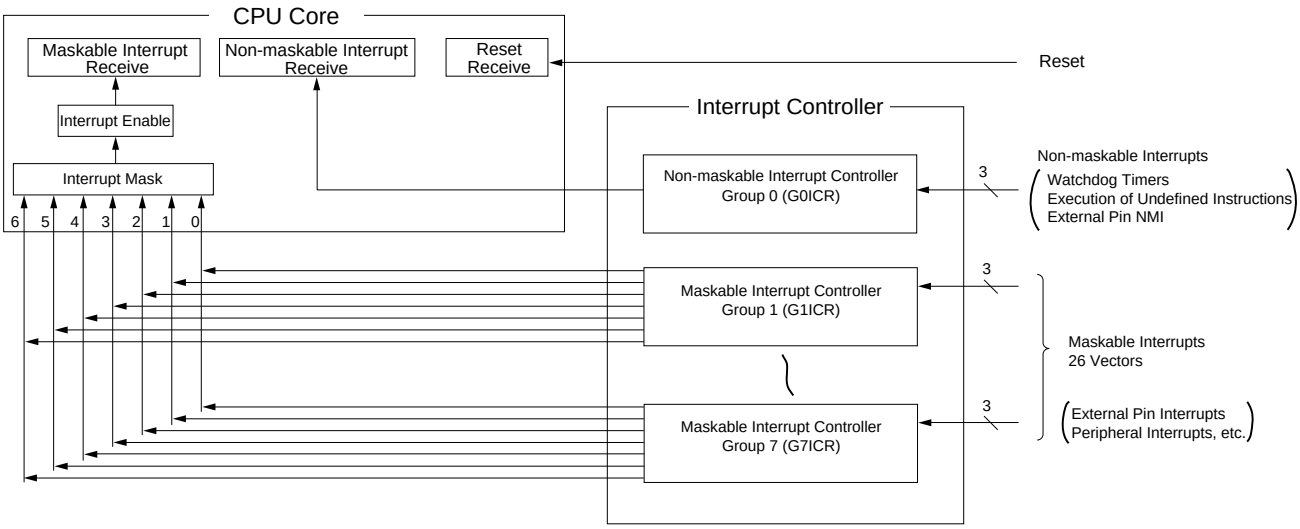


Figure 1-1-2 Interrupt Controller Configuration

The CPU checks the processor status word to determine whether an interrupt request is accepted or not. When an interrupt is accepted, automatic servicing by hardware starts and the program counter and PSW are pushed to the stack. Next, the program moves to the interrupt. After specifying the interrupt vector, it branches to the entry address of the interrupt service for that interrupt.

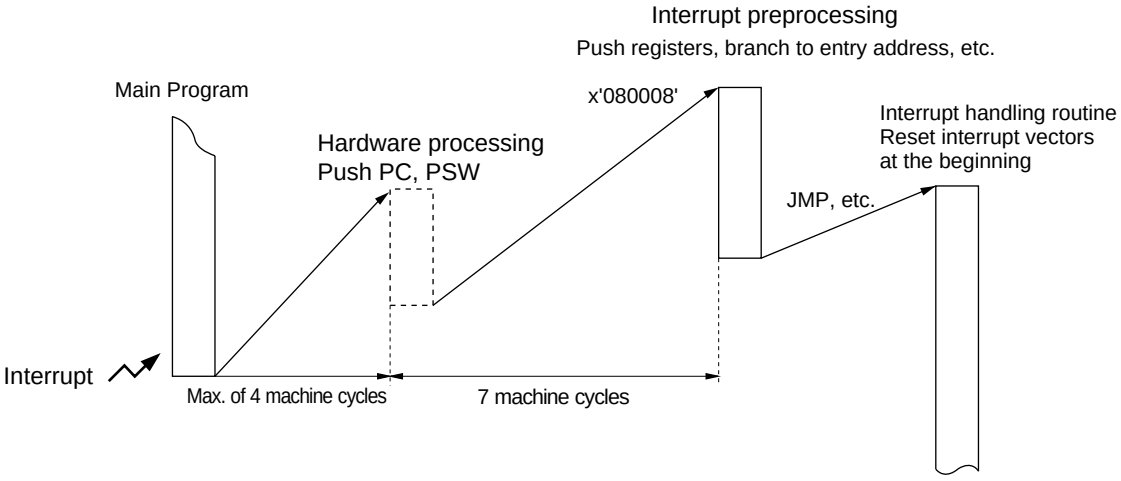


Figure 1-1-3 Interrupt Servicing Sequence

1-2 Basic Specifications

This section describes the basic specification of this series. Please refer to Product Standards for details.

Table 1-2-1 Basic Specifications (1/2)

CPU Structure	Load/store architecture Eight registers: Four 24-bit data registers Four 24-bit address registers Others : 24-bit program counter 16-bit processor status word 16-bit multiplication/division register
Instruction	36 instructions 6 addressing modes One-byte primitive instruction length Code assignment: 1 to 2 bytes (Basic) + 0 to 3 bytes (Extension)
Basic Performance	10 MHz internal operating frequency with a 20-MHz oscillator and internal 4x-speed Clock cycles: For instruction execution, minimum 1 cycle (100 ns) For register-to-register operations, minimum 1 cycle For load/store operations, minimum 1 cycle For conditional branching operations, 1 to 3 cycles
Pipeline	3 stages: Instruction fetch, decode, execute
Address Space	16-MB linear address space
External Bus	Address 24 bits 4 $\overline{CS}$ signals Data 8/16-bit Minimum bus cycle 1 cycle (at 100 ns / 20 MHz) Bus width and wait cycle is set in 4 MB unit. (Selectable from handshake or fixed bus wait mode) ROM burst mode support Selectable from either address/data separate pin or address/data share pin.
Low-power Mode	SLOW mode, STOP mode, HALT mode
Frequency Circuit	High-speed: max. 22.6 MHz, Low-speed: 32 kHz

Table 1-2-1 Basic Specifications (2/2)

Interrupt	26 vectors 3 non-maskable interrupts 23 maskable interrupts (7 interrupt priority level settings) External interrupts 5 external interrupts (individual IRQ, edge specification) 1 external non-maskable interrupt 20 internal interrupts 12 timer interrupts, 4 serial interrupts, 1 ATC interrupt, 1 A/D interrupt, 1 watchdog timer interrupt, 1 undefined instruction interrupt
Timer/Counter	Six 8-bit timers (down counters) Reload timer Cascading function (serve as 16 to 40 bit timers, as well) Timer output (duty of 1:1) Internal clock source or external clock source Serial interface clock generation Start timing generation for A/D converter Two 16-bit timers (two up-down counters) 2 channels compare/capture registers Internal clock source or external clock source Timer output (duty of 1:1) (max: 4) PWM/one-shot pulse output (max.: 2) 2-phase encoder input (x4, x1) 17-bit watchdog timer
ATC*	1 channel (Fixed between serial channel 0 to internal RAM) Transfer request : serial (channel 0) transmission/reception interrupt request Transfer rate : 600 ns (1 byte data transfer rate at 20 MHz oscillating)
Serial Interface	2 UART/synchronous (shared) serial interfaces
Analog Interface	A/D converter Eight 8-bit inputs Auto scanning (1 to 8 channel settings)
Byte Swap Register	2-byte, 3-byte and 4-byte swap are available.
I/O Port	80 I/O ports (All shared pins except ROM less model) 48 I/O ports (All shared pins of ROM less model)
Package	100-pin LQFP pitch: 0.5 mm dimension: 14-mm-square

Note) ATC stands for Auto Transfer Control. Refer to chapter 7 ATC for details.

1-3 Block Diagram

Figure 1-3-1 shows the block diagram including the CPU core and Table 1-3-1 describes the block functions.

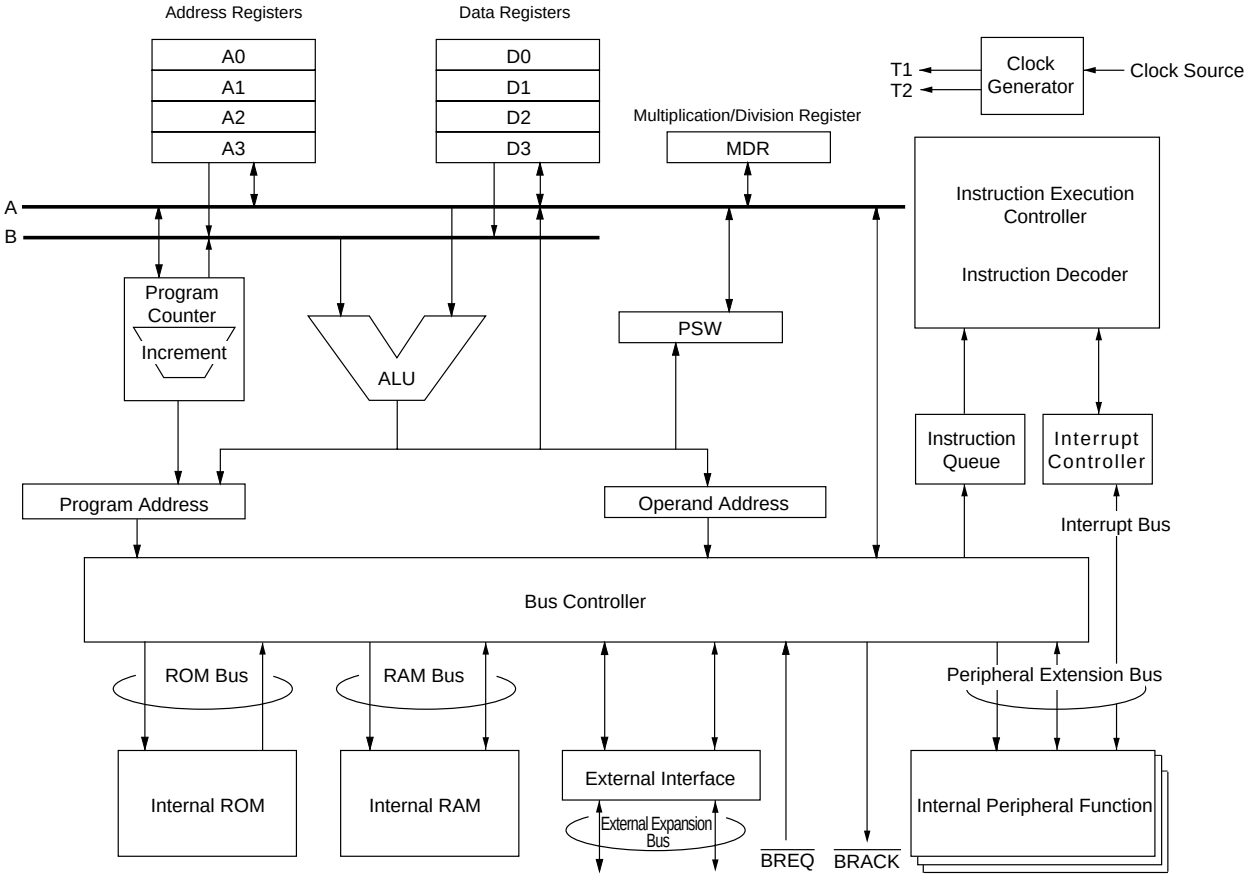
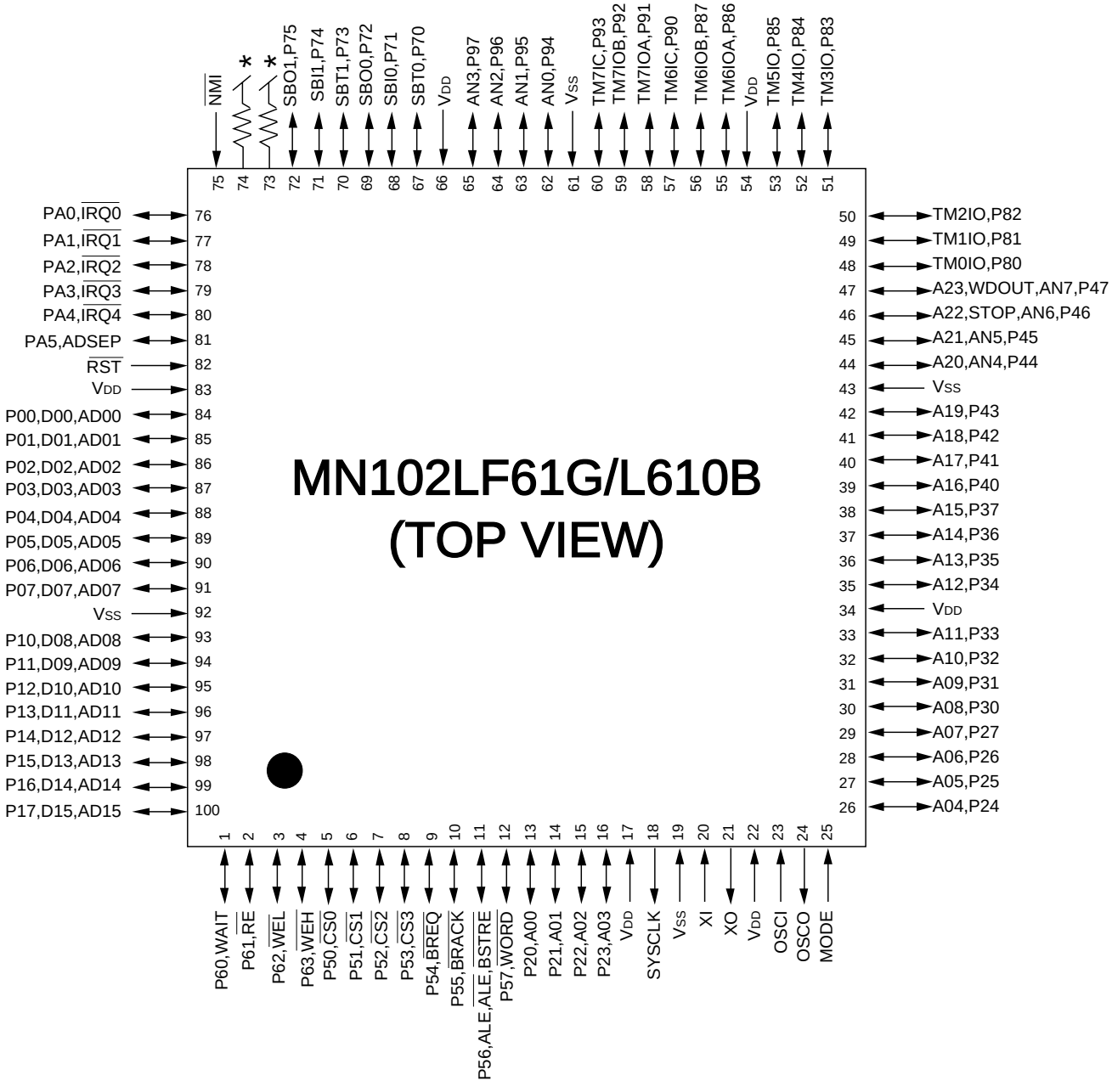


Figure 1-3-1 Block Diagram

Table 1-3-1 Block Functions

Block	Functions
Clock Generator	The clock generator contains the clock oscillation circuit connected to an external crystal and supplies the clock to all CPU blocks. (It has a built-in 4x-speed circuit.)
Program Counter	The program counter generates addresses for instruction queues. Normally, it gets increments based on the sequencer indication, but for branch instructions and interrupt acceptance, it sets the branch address or ALU operation results.
Instruction Queue	The instruction queue saves up to 4 bytes of prefetched instructions.
Instruction Decoder	The instruction decoder decodes the instruction queue content, generates control signals needed for the instruction execution, and executes the instruction by controlling each block in the CPU.
Instruction Execution Controller	The instruction execution controller controls the operations of each CPU function based on results from the instruction decoder and interrupt requests.
ALU	The ALU calculates the operand addresses for arithmetic operations, logic operations, shift operations, register relative indirect, indexed addressing and register indirect addressing mode.
Internal ROM, Internal RAM	Internal ROM and internal RAM are allocated as the execution program, data and stack areas.
Address Registers (An)	The address registers (An) store the addresses of memory accessed during data transfer. They also store the base addresses in the register relative indirect, indexed addressing and register indirect addressing mode.
Operation Registers (Dn, MDR)	The data registers (Dn) store the operation results and transfer the data to memory. They also store the offset addresses in indexed addressing and register indirect addressing mode. The multiplication/division register (MDR) stores the data for multiplication/division operations.
PSW	The processor status word (PSW) stores the flags that indicate the status of the CPU interrupt controller and operation results.
Interrupt Controller	The interrupt controller detects the interrupt requests from the peripheral functions, and requests the CPU to move to the interrupt handling.
Bus Controller	The bus controller controls the connection between the CPU internal bus and the CPU external bus. It also contains the bus arbitration function.
Internal Peripheral Function	This series contains the peripheral functions including timers, serial interface, A/D converter and so on.

1-4 Pin Description



* : Use 33 kΩ to 50 kΩ.

Figure 1-4-1 Pin Configuration

The unused input pins are connected to VDD/VSS, the unused output pins are opened and the unused I/O pins are connected to VDD/VSS by setting the direction in ports or opened.

1-4-1 List of Pin Functions

Refer to “9-2-3 List of Pin Functions” for each pin’s input level, and Schmitt and pull-up resistor availability. TTL in the input level column means that the input is determined at TTL level. CMOS in the input level column means that the input is determined at CMOS level. The column with “yes” sign shows Schmitt, while the column with no mark shows no Schmidt. Pull-up resistors are in the column with “yes”. The column with “programmable” can be set by pull-up control registers (PPLU). Please see “Chapter 8 Ports” for details.

Table 1-4-1 List of Pin Functions (1/9)

Pin Name	Input/Output	Shared Pin	Function	Description
V_{DD}	—	—	Power	There are six V_{DD} pins. Connect these six pins to a power supply of 4.5 V to 5.5 V.
V_{SS}	—	—	Power (Ground)	There are four V_{SS} pins. Connect these four pins to a power supply of 0 V.
OSCI OSCO	Input Output	— —	High-speed Oscillator Input (4 to 22.6 MHz) High-speed Oscillator Output (4 to 22.6 MHz)	For a self-excited oscillator configuration, connect crystal or ceramic oscillator across these two pins. They have a built-in feedback resistor between them. For stability, insert capacitor of 20 pF to 33 pF between the OSCI or OSCO pin and V_{SS} pin. (For the exact capacitance, consult the oscillator manufacturer.) [☞ Figure 1-4-2 OSCI and OSCO Connection Example] For an external oscillator configuration, connect the OSCI pin to an oscillator with an amplitude of 4 to 22.6 MHz at the width between V_{DD} and V_{SS}. Leave the OSCO open. Connecting the OSCO pin with the external circuit is not allowed. Select the SYSCLK pin as a synchronous signal.
XI XO	Input Output	— —	Low-speed Oscillator Input (32 kHz to 200 kHz) Low-speed Oscillator Output (32 kHz to 200 kHz)	For a self-excited oscillator configuration, connect crystal or ceramic oscillator across these two pins. They have a built-in feedback resistor between them. For stability, insert capacitor of 100 pF to 200 pF between the XI pin or the XO pin and the V_{SS} pin (For the exact capacitance, consult the oscillator manufacturer). [☞ Figure 1-4-3] For an external oscillator configuration, connect the XI pin to an oscillator with an amplitude of 32 kHz to 200 kHz and the width between V_{DD} and V_{SS}. Leave the XO pin open. [☞ Figure 1-4-3] If the XI pin is not used, connect it to V_{SS} or V_{DD}. If the XO pin is not used, leave it open. Select the SYSCLK pin for a synchronous signal.

Table 1-4-1 List of Pin Functions (2/9)

Pin Name	Input/Output	Shared Pin	Function	Description
$\overline{\text{RST}}$	Input	—	Reset Input	This pin resets the chip. With a 20-MHz oscillator, reset starts when the low level is input to this pin for more than 400 ns. Reset may start even when the noise is input to this pin for less than 400 ns, so please pay highly attention to noise. Reset is released when the high level is input to the pin. The oscillation waits of the high-speed oscillation pin (OSCI) are performed (approximately 6 ms to 7 ms with a 20-MHz oscillator). After that, the chip starts executing the instruction from x"080000". [☞ Figure 1-4-4 Reset Connection Example]
SYSCLK	Output	—	System Clock Output	This pin provides the system clock. After reset release, the oscillation waits of OSCI are always performed and this pin outputs the clock of 10 MHz at a 20-MHz oscillation. Please keep in mind that this pin holds the high level until the oscillation waits are released after the $\overline{\text{RST}}$ pin becomes the low level.
MODE	Input	—	Memory Mode Input	This pin sets either processor mode or single-chip mode (memory expansion mode). Pulling the pin low sets the processor mode. In processor mode, internal ROM becomes the external memory area. Pulling the pin high sets the single-chip mode (memory expansion mode). [☞ Chapter 2-1-1, 2-2-3 Memory expansion mode] Do not change the mode setting in this pin during operation. When the setting is changed, proper operation is not guaranteed. For ROM less model, set this pin to “L”.
P57	I/O	$\overline{\text{WORD}}$	General-purpose port 5 Data Bus Width Input	This pin can be used as a general-purpose input/output port (only in single-chip mode.) [☞ Chapter 8 Ports] This pin sets the data bus size of block 0 (x’010000’ to x’3FFFFF’), which obtained by dividing 16-byte space into four (0 to 3), to either 8-bit data bus width or 16-bit data bus width in processor mode or memory expansion mode. (Bus width of internal ROM, RAM and special function registers are always 16-bit width.) Setting this pin to “L” level selects 16-bit data bus width, and Setting this pin to “H” level selects 8-bit data bus width. In processor mode and memory expansion mode, always use this pin as data bus width input pin. If bus width is changed during operation, proper operation is not guaranteed.

Table 1-4-1 List of Pin Functions (3/9)

Pin Name	Input/Output	Shared Pin	Function	Description
P54 P55	I/O Input I/O Output	$\overline{BREQ}$ $\overline{BRACK}$	General-purpose Port 5 Bus request General-purpose Port 5 Bus request enable output	These pins can be used as general-purpose input/output ports. [☞ Chapter 8 Ports] $\overline{BREQ}$ and $\overline{BRACK}$ pins operate bus arbitration. Pulling $\overline{BREQ}$ low suspends the execution of the current instruction, releases bus and sets $\overline{BRACK}$ to "L" level. While the chip is accessing the bus, the chip releases the bus after the bus access is completed, and sets $\overline{BRACK}$ to "L" level. Pulling $\overline{BREQ}$ high at the level detector restores the bus. [☞ Chapter 2-2-2 Example of External Memory Connection]
P62 P63 P61	I/O Output I/O Output I/O Output	$\overline{WEL}$ $\overline{WEH}$ $\overline{RE}$	General-porpose port6 Lower Byte Write Enable Output General-porpose port6 Upper Byte Write Enable Output General-porpose port6 Read Enable Output	These pins can be used as general-purpose input/output ports. [☞ Chapter 8 Ports] These pins provide a control signal for the memory read/write. When connecting SRAM and ROM, connect $\overline{RE}$ to $\overline{OE}$ in memory. $\overline{RE}$ outputs low level during read and read out the data of memory. When connecting SRAM, connect $\overline{WEL}$ and $\overline{WEH}$ to $\overline{WE}$ in memory. $\overline{WEL}$ and $\overline{WEH}$ output low level during write and write the data to memory. $\overline{WEH}$ controls write to D15-D08, $\overline{WEL}$ controls write to D07-D00. $\overline{WEL}$ is invalid when 8-bit bus width is selected in memory expansion mode so that it can be used as a general-purpose port. In processor mode these pins serve as $\overline{WEL}$, $\overline{WEH}$ and $\overline{RE}$. (cannnot be used as general-purpose ports.) During a bus request (when $\overline{BREQ}$ is "L"), STOP mode or HALT mode, these pins will be in a high impedance state. (but they do not become high impedance state when used as ports. [☞ Chapter 2-2-2, 2-2-4 Example of External Memory Connection]

Table 1-4-1 List of Pin Functions (4/9)

Pin Name	Input/Output	Shared Pin	Function	Description
P43-P40	I/O		General-purpose Port 4	These pins can be used as general-purpose input/output ports. [☞ Chapter 8 Ports]
	Output	A19-A16	Address output	These pins output memory address (A19-A16) in memory expansion mode and processor mode, and are connected to memory address pin or address decoder circuit. Address output at the timing when these pins do not access to the memory is indifined (it outputs some fixed value). In processor mode, these pins serve as A19-A16. (cannnot be used as general-purpose input/output ports.) During a bus request (when $\overline{BREQ}$ is "L"), STOP mode or HALT mode, these pins will be in a high impedance state. (but they do not become high impedance state when used as ports.)
P45-P44	I/O		General-purpose Port 4	When these pins are used as general-purpose input/output ports, I/O direction control is in bit unit.
	Input	AN5-AN4	A/D converter input	These serve as input pins for A/D converter. [☞ Chapter 6 Analog interface].
	Output	A21-A20	Address output	These pins output memory address (A21-A20) in memory expansion mode and processor mode, and are connected to memory address pin or address decoder circuit. Address output at the timing when these pins do not access to the memory is indifined (it outputs some fixed value). In processor mode, these pins serve as A21-A20. (cannnot be used as general-purpose input/output ports.) During a bus request (when $\overline{BREQ}$ is "L"), STOP mode or HALT mode, these pins will be in a high impedance state. (but they do not become high impedance state when used as ports.)

Table 1-4-1 List of Pin Functions (5/9)

Pin Name	Input/Output	Shared Pin	Function	Description
P46	I/O		General-purpose Port 4	When this pin is used as general-purpose input/ output ports, I/O direction control is in bit unit.
	Input	AN6	A/D converter input	This is a input pin for A/D converter. [☞ Chapter 6 Analog interface].
	Output	STOP	STOP status signal	In STOP or HALT mode, This pin becomes “H” level.
	Output	A22	Address output	This pin outputs memory address (A22) in memory expansion mode and processor mode, and is connected to memory address pin or address decoder circuit. Address output at the timing when this pin does not access to the memory is indifined (it outputs some fixed value). During a bus request (when $\overline{\text{BREQ}}$ is “L”), STOP mode or HALT mode, this pin will be in a high impedance state. (but this pin does not become high impedance state when used as ports.)
P47	I/O		General-purpose Port 4	When this pin is used as general-purpose input/ output ports, I/O direction control is in bit unit.
	Input	AN7	A/D converter input	This is a input pin for A/D converter. [☞ Chapter 6 Analog interface].
	Output	WDOUT	Watchdog Timer Overflow Signal	When the watchdog timer is overflowed, pulse is output.
	Output	A23	Address output	This pin outputs memory address (A23) in memory expansion mode and processor mode, and is connected to memory address pin or address decoder circuit. Address output at the timing when this pin does not access to the memory is indifined (some fixed value). During a bus request (when $\overline{\text{BREQ}}$ is “L”), STOP mode or HALT mode, this pin will be in a high impedance state. (but this pin does not become high impedance state when used as ports.)

Table 1-4-1 List of Pin Functions (6/9)

Pin Name	Input/Output	Shared Pin	Function	Description
P37-P30	I/O		General-purpose Port 3	When these pins are used as general-purpose input/output ports, I/O direction control is in bit unit. [☞ Chapter 8 Ports]
	Output	A15-A08	Address output	These pins output memory address (A15-A08) in memory expansion mode and processor mode, and are connected to memory address pin or address decoder circuit. Address output at the timing when these pins do not access to the memory is indifined (it outputs some fixed value). In processor mode, these pins serve as A15-A08. (cannnot be used as general-purpose input/output ports.) During a bus request (when $\overline{\text{BREQ}}$ is “L” level), STOP mode or HALT mode, these pins will be in a high impedance state. (but they do not become high impedance state when used as ports.)
P27-P20	I/O		General-purpose Port 2	When these pins are used as general-purpose input/output ports, I/O direction control is in bit unit. [☞ Chapter 8 Ports]
	Output	A07-A00	Address output	These pins output memory address (A07-A00) in memory expansion mode and processor mode, and are connected to memory address pin or address decoder circuit. Address output at the timing when these pins do not access to the memory is indifined (it outputs some fixed value). In processor mode, these pins are A07-A00. (cannnot be used as general-purpose input/output ports.) During a bus request (when $\overline{\text{BREQ}}$ is “L” level), STOP mode or HALT mode, these pins will be in a high impedance state. (but they do not become high impedance state when used as ports).

Table 1-4-1 List of Pin Functions (7/9)

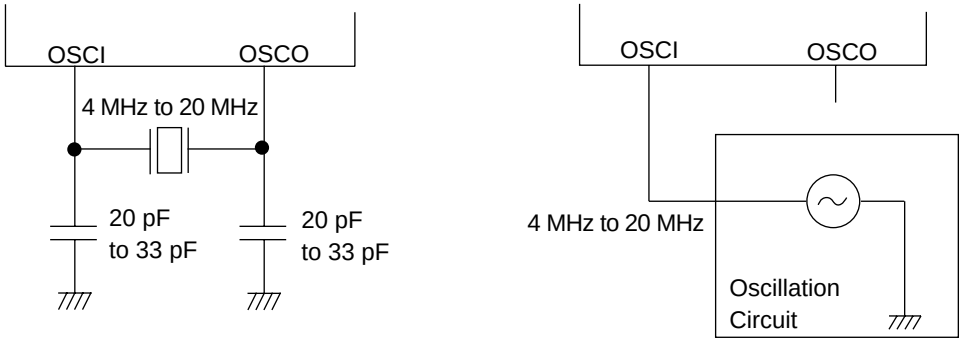
Pin Name	Input/Output	Shared Pin	Function	Description
P17-P10 P07-P00	I/O I/O	 D15-D00 (AD15- AD00)	General-purpose Port 1, 0 Data (address/data) Input/output	When these pins are used as general-purpose input/output ports, I/O direction control is in bit unit. [☞ Chapter 8 Ports] In processor mode or memory expansion mode, these pins provide data input or output during address/data separate mode, and provide memory address output (lower 16-bit) and data input or output in time-sharing in address/data share mode. These pins serve as input pins when the external memory is not accessed. [☞ Chapter 2-2-2, 2-2-4 Example of External Memory Connection] During a bus request (when $\overline{BREQ}$ is “L” level), STOP mode or HALT mode, these pins will be in a high impedance state.(but they do not become high impedance state when used as ports.)
P53-P50	I/O Output	$\overline{CS3}$-$\overline{CS0}$	General-purpose Port 5 Chip Select Output	When these pins are used as general-purpose input/output ports, I/O direction control is in bit unit. [☞ Chapter 8 Ports] When connect ROM and SRAM, connect $\overline{CS3-0}$ to $\overline{CS}$ pin in the memory. For memory map of $\overline{CS3-0}$ in address space, refer to [☞ Chapter 2 Bus Interface]. Note that $\overline{CS0}$ is not output during internal ROM access. During a bus request (when $\overline{BREQ}$ is “L” level), STOP mode or HALT mode, these pins will be in a high impedance state.(but they do not become high impedance state when used as ports.)
PA5	I/O Input	 ADSEP	General-purpose Port A Address/data separate or share mode setup	These pins can be used as general-purpose input or output port. (only in single-chip mode) [☞ Chapter 8 Ports] In processor mode or memory expansion mode, this pin selects address/data separate mode or address/data share mode. Setting this pin to “H selects address/data separate mode and setting this pin to “L” selects address/data share mode. Use this pin always as address/data separate mode or address/data share setup pin in processor mode or memory expansion mode. If the setup is changed during operation, proper operation is not guaranteed.

Table 1-4-1 List of Pin Functions (8/9)

Pin Name	Input/Output	Shared Pin	Function	Description
P56	I/O Output	 $\overline{\text{BSTRE}}$ (ALE/$\overline{\text{ALE}}$)	General-purpose Port 5 Read Enable Output for Burst ROM (address latch enable output)	This pin can be used as general-purpose input/output port. [☞ Chapter 8 Ports] In memory expansion mode, this port provides RE signal for burst ROM in address/data separate mode. (Note that this pin does not need to be connected to burst ROM with penalty as normal RE pin, instead, can be connected to the burst ROM with penalty.) [☞ Chapter 2-1-3 ROM Burst Mode Timing] In address/data share mode, this pin outputs the timing that address output to AD15-0 is latched outside. Note that ALE is positive logic at reset release and can be switched to negative logic with register setting, thus, negative logic cannot be used in processor mode. Note that ALE could be output even in the cycle that does not access to external device. During a bus request ($\overline{\text{BREQ}}$ is “L” level), STOP mode or HALT mode, this pin will be in a high impedance state.(but it does not become high impedance state when used as ports.)
P60	I/O Input	 WAIT	General-purpose Port 6 Bus Cycle Wait Input	This pin can be used as general-purpose input/output port. [☞ Chapter 8 Ports] When external memory is in handshake mode, this pin provides signal that extend the access cycle to the external memory. When “L” level is input to this signal, external memory access ends. [☞ Figure 1-4-5]
P74, P71 P75, P72	I/O Input I/O Output	 SBI1-0 SBT1-0	General-purpose Port 7 Serial Interface Data Input General-purpose Port 7 Serial Interface Data Output	This pin can be used as general-purpose input/output port. [☞ Chapter 8 Ports] These are data input /output pins for serial interface. When these pins are unused, fix the input pin to “H” level and leave the output pin open. [☞ Chapter 5 serial interface]
P70 P73	I/O I/O I/O I/O	 SBT0 SBT1	General-purpose Port 7 Serial Interface 0 Clock Input/output General-purpose Port 7 Serial Interface 1 Clock Input/output	This pin can be used as general-purpose input/output port. [☞ Chapter 8 Ports] When used with serial interface, these pins provide synchronous transfer clock signal. When these pins are unused, fix the input pin to “H” level and leave the output pin open. [☞ Chapter 5 serial interface]

Table 1-4-1 List of Pin Functions (9/9)

Pin Name	Input/Output	Shared Pin	Function	Description
P85-P80	I/O I/O	TM5IO-TM0IO	General-purpose Port 8 Timer 5-0 Input/output	When these pins are used as general-purpose input/output ports, I/O direction control is in bit unit. [☞ Chapter 8 Ports] They are input/ouput pins for timer 5-0
P86	I/O I/O	TM6IOA	Timer 6A Input/output	This pin can be used as general-purpose input/output port. This pin serves as timer input capture input pin and ouput compare output pin.
P87	I/O I/O	TM6IOB	Timer 6B Input/output	This pin can be used as general-purpose input/output port. This pin serves as timer input capture input pin and ouput compare output pin.
P90	I/O Input	TM6IC	Timer 6 Counter Clear	This pin can be used as general-purpose input/output port. This pin serves as timer 6 counter clear. [☞ Chapter 4 Timer Counter]
P91	I/O I/O	TM7IOA	Timer 7A Input/output	This pin can be used as general-purpose input/output port. This pin serves as timer input capture input pin and ouput compare output pin.
P92	I/O I/O	TM7IOB	Timer 7B Input/output	This pin can be used as general-purpose input/output port. This pin serves as timer input capture input pin and ouput compare output pin.
P93	I/O Input	TM7IC	Timer 7 Counter Clear	This pin can be used as general-purpose input/output port, and when used as general-purpose port, it can be used as LED driver port. This pin serves as timer 7 counter clear. [☞ Chapter 4 Timer Counter]
P97-P94	I/O Input	AN3-AN0	General-purpose Port 9 A/D Converter Input	When these pins are used as general-purpose input/output ports, I/O direction control is in bit unit. These are A/D converter input pins. [☞ Chapter 6 Analog Interface] When P94 is used as a general-purpose port, it can be used as LED driver port.
$\overline{\text{NMI}}$	Input		$\overline{\text{NMI}}$	An $\overline{\text{NMI}}$ interrupt occurs on the falling edge to low level at negative logic. (When reading the PortA, the pin value can be monitored at bit 6.)
PA4-0	I/O Input	$\overline{\text{IRQ4}}$-$\overline{0}$	General-purpose Port A External Interrupt	When these pins are used as general-purpose input/output ports, I/O direction control is in bit unit. [☞ Chapter 8 Ports]



(Note)Capacity varies depending on the crystal oscillator.

Figure 1-4-2 OSCI and OSCO Connection Example

Figure 1-4-3 XI, XO Connection Example

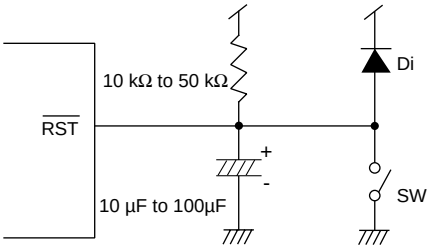


Figure 1-4-4 Reset Connection Example

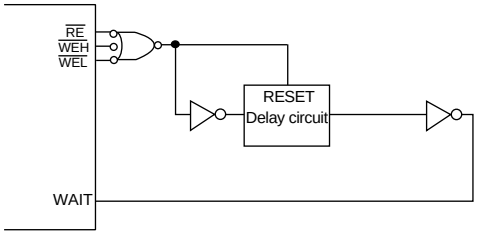
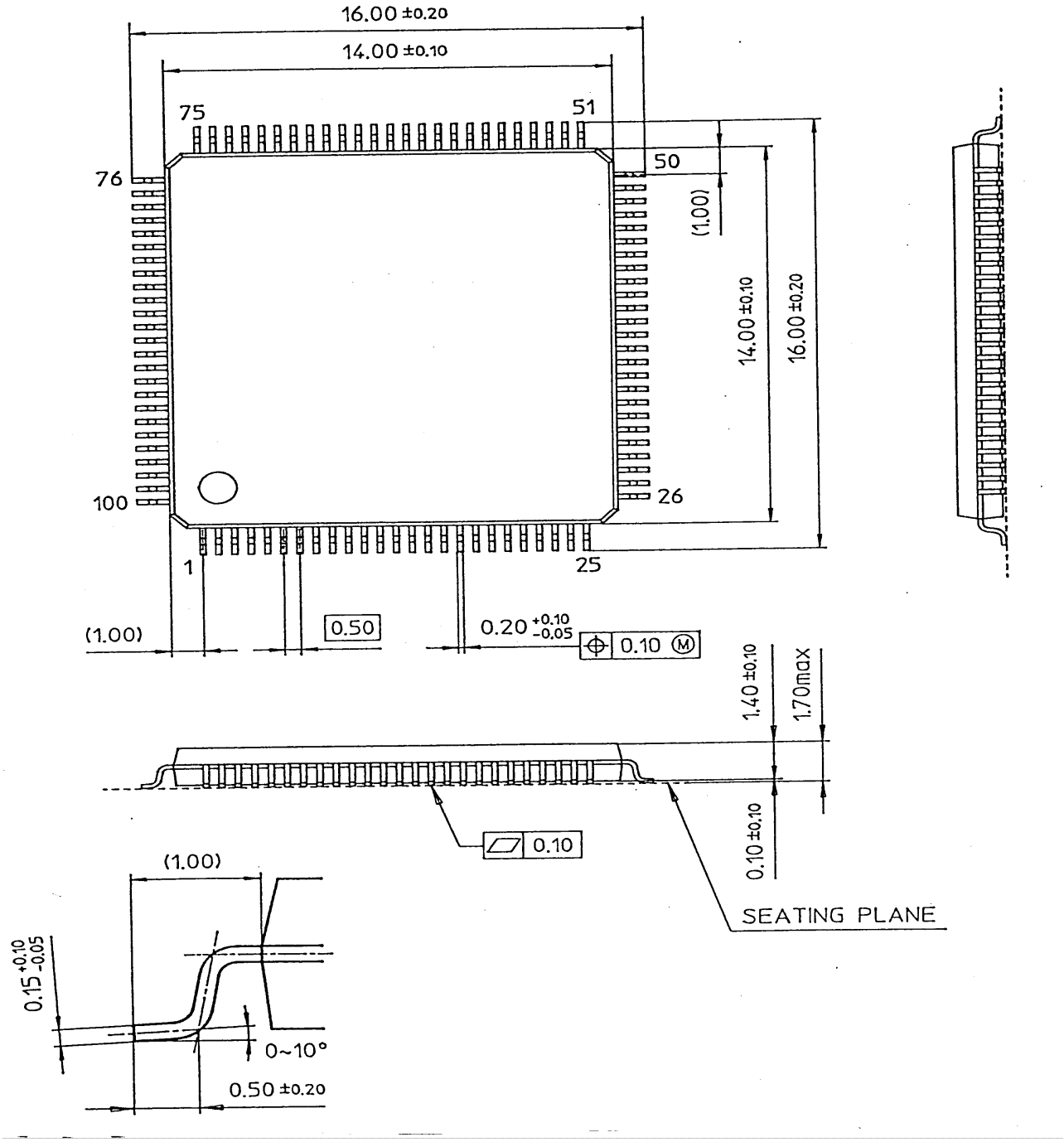


Figure 1-4-5 WAIT Signal Control Circuit Example

1-5 Package Dimension

Package Code: LQFP100-P-1414 unit: mm



Body Material: Epoxy Resin, Lead Material: Cu Alloy, Lead Finish Method: Pd Plating

Figure 1-5-1 100-pin LQFP (14 mm square)

The package dimension is subject to change. Before using this product, please obtain product specifications from the sales office.

Chapter 2 Bus Interface

2

2-1 Bus Interface

2-1-1 Overview

The MN102L610B has only processor mode.

This series contains three memory modes of single-chip mode, memory expansion mode and processor mode. The chip of this series connects to the external memory or I/O consisted of gate array in the expansion mode or processor mode. The address space is divided into four fixed areas (Block 0 to Block 3). Each block has approximately 4 MB area and generates four chip-select signals to its corresponding external space. (The address space is optionally divided when the chip-select signals are generated externally.)

16-bit bus width or 8-bit bus width is selected for each block. The $\overline{\text{WORD}}$ pin sets the 16-bit bus width or 8-bit bus width for Block 0 where the reset handler exists. On the other hand, the MEMMDn register sets the bus width for Block 1 to Block 3. See 1-4 Pin Functions for pin setting.

* MN102L610B does not contain internal ROM.

* Accessing the virtual area using the program means accessing the real area in this series.

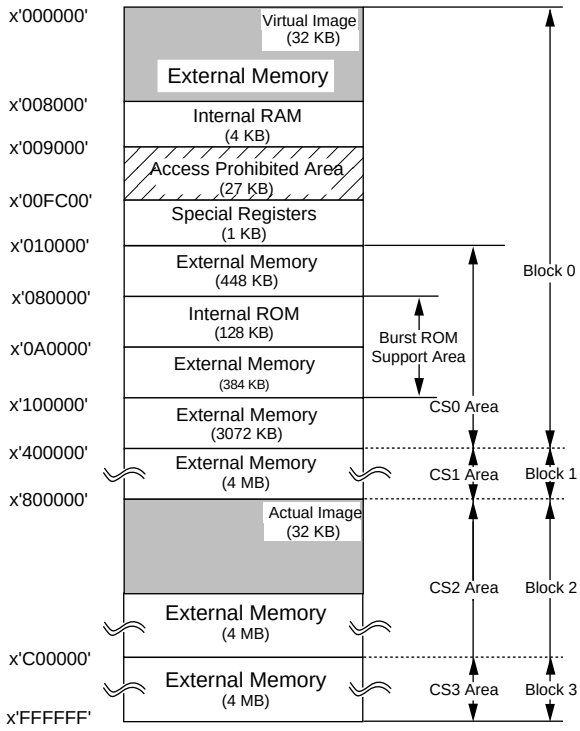


Figure 2-1-1 Address Space

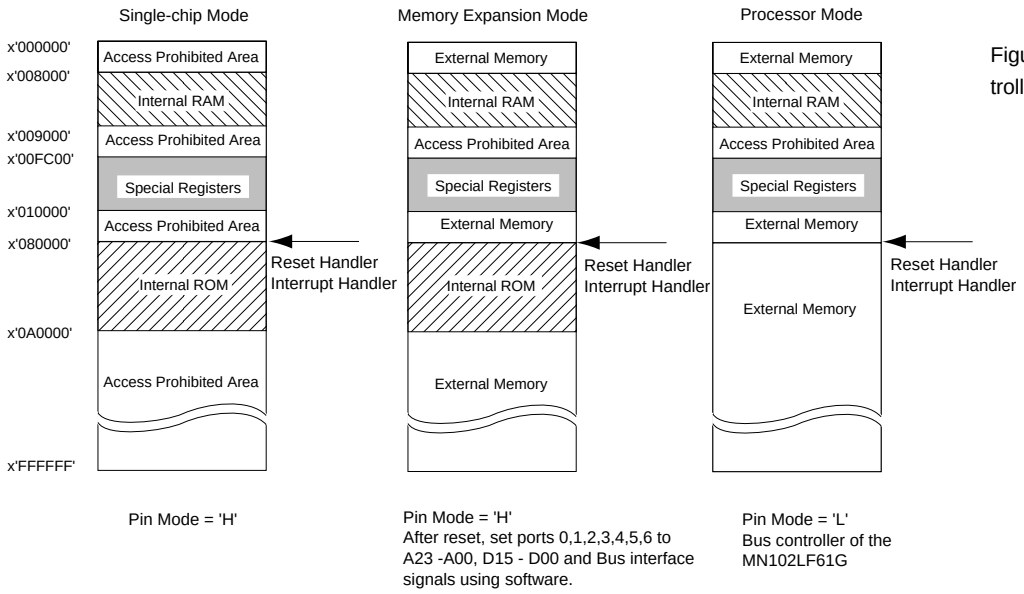


Figure 2-1-2 shows the bus controller of the MN102LF61G.

Figure 2-1-2 Bus Controller

In this series, the addresses of x'000000' to x'007FFF' replaces the addresses of x'800000' to x'807FFF'. Beacuse of this, the CS2 signal is generated even though the program accesses the address of x'000000' to x'007FFF' shown in Figure 2-1-1. The CS1 pin, CS2 pin and CS3 pin are allocated into Block1, Block2 and Block 3 respectively, and these pins become low level.

CS0	x'010000' to x'3FFFFF' (The CS0 signal is not generated in the internal ROM area.)
CS1	x'400000' to x'7FFFFF'
CS2	x'000000' to x'007FFF' x'800000' to x'BFFFFF'
CS3	x'C00000' to x'FFFFFF'

The CS0 signal is generated even in the internal ROM area during processor mode.

Accessing the logical addresses of x'000000' to x'007FFF' means accessing the addresses of x'800000' to x'807FFF'.

Table 2-1-1 CS Signal Generation

This series has two modes of address/data shared mode and address/data separated mode. The ADSEP pin selects each mode. Figure 2-1-3 to Figure 2-1-7 show the pin configuration in each mode.

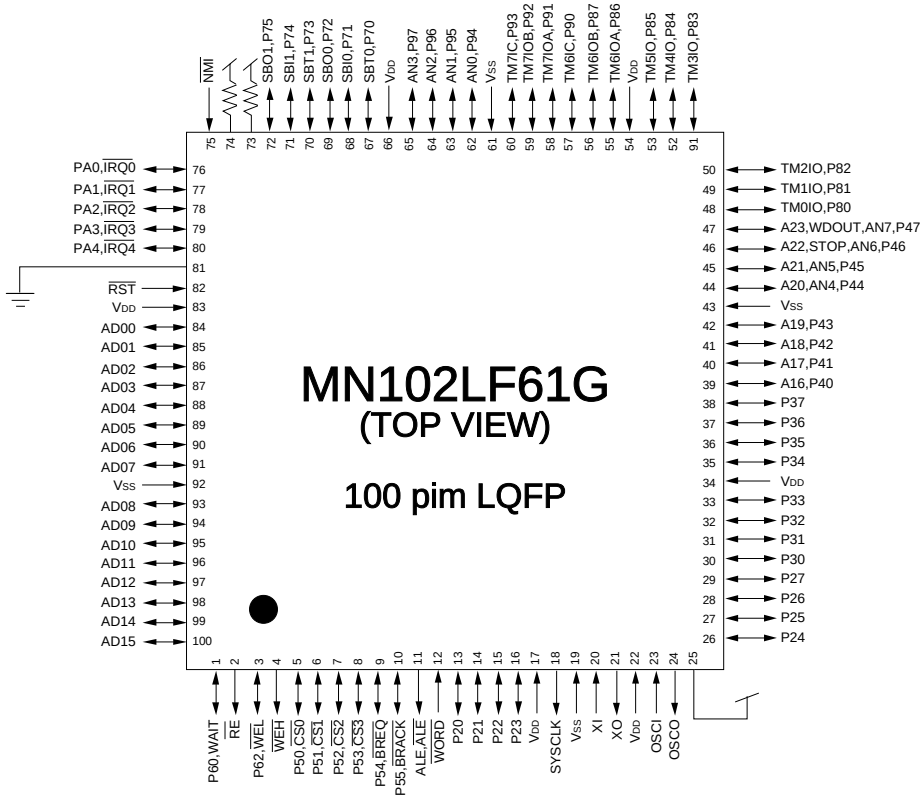


Figure 2-1-3 Memory Expansion Mode (Address/Data Shared Pin Configuration)

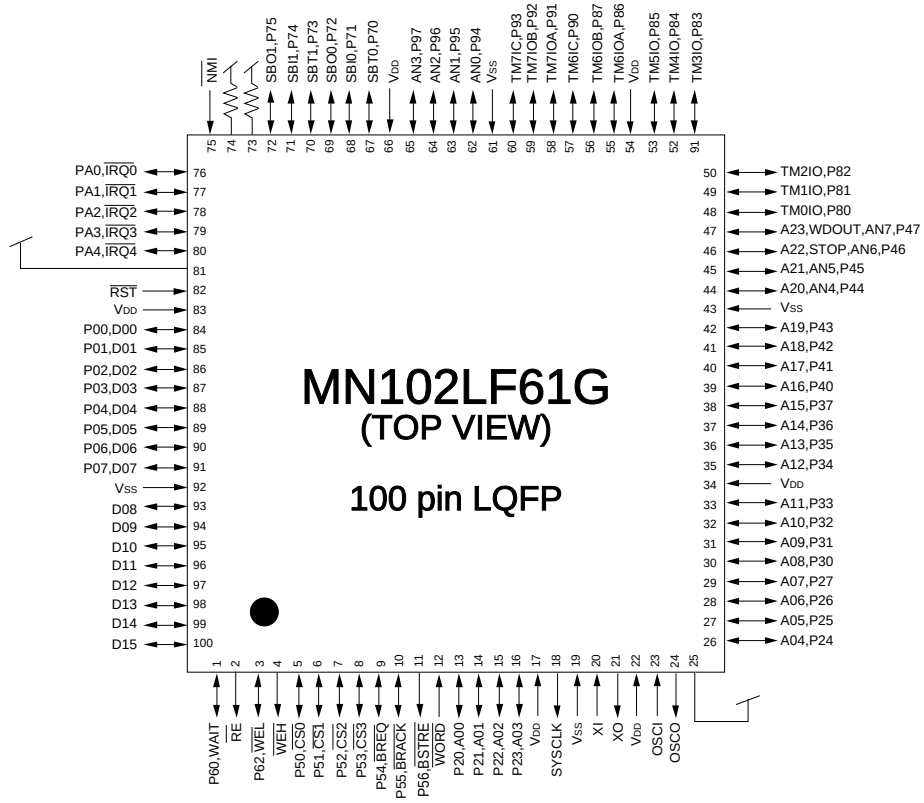


Figure 2-1-4 Memory Expansion Mode (Address/Data Separated Pin Configuration)

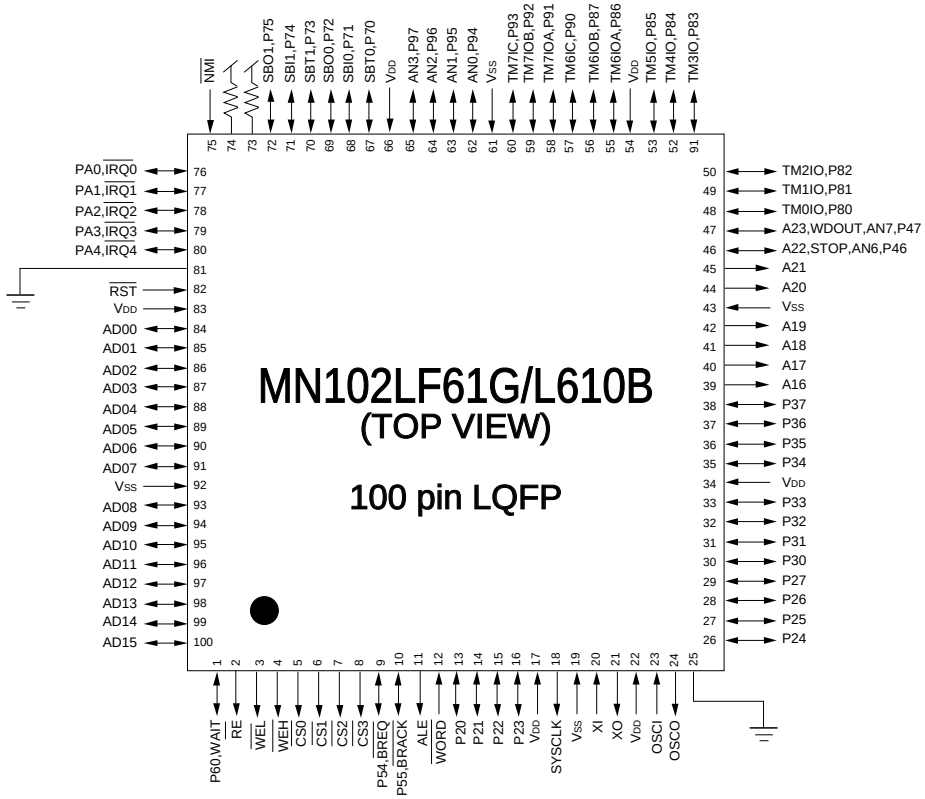


Figure 2-1-5 Processor Mode
(Address/Data Shared Pin Configuration)

Pin configurations of MN102L-610B are Figure.2-1-5, and 2-1-6.

$\overline{ALE}$ is not generated during processor mode.

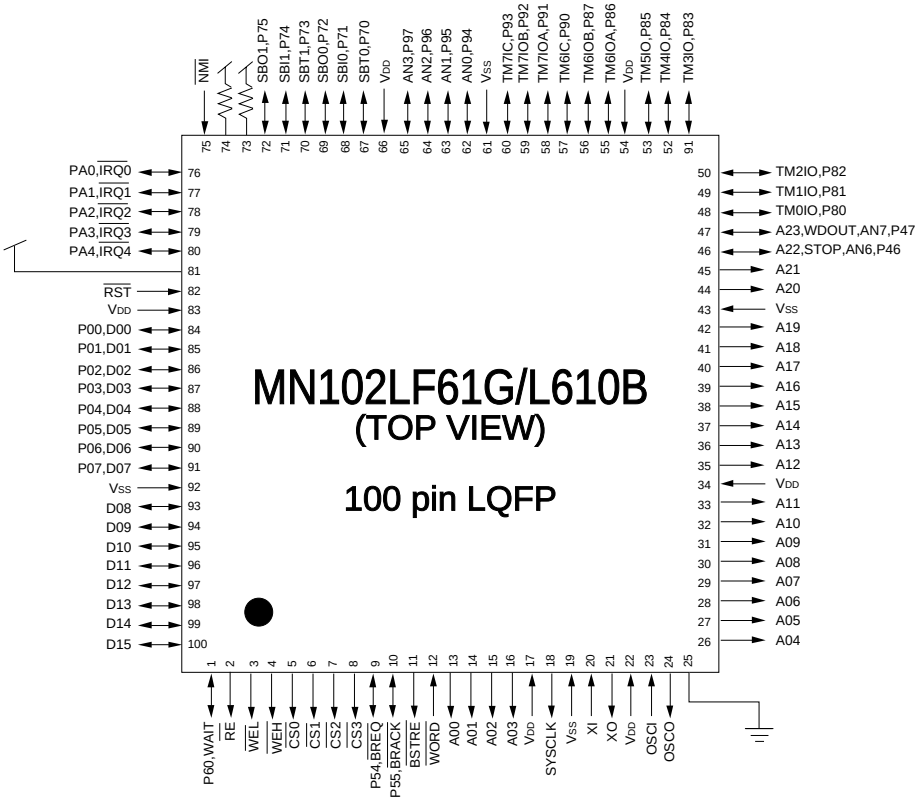


Figure 2-1-6 Processor Mode
(Address/Data Separated Pin Configuration)

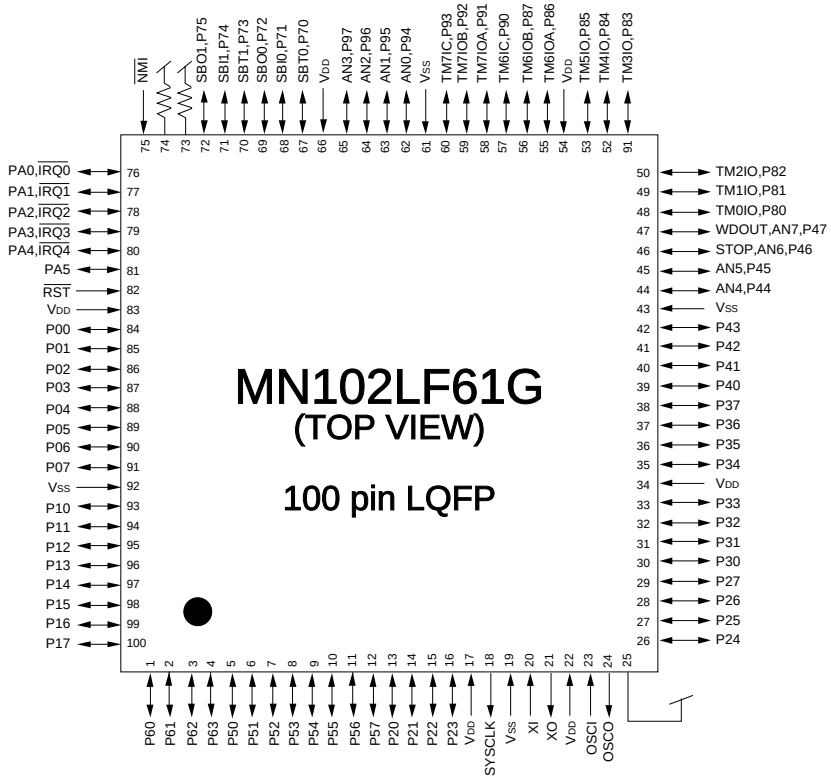


Figure 2-1-7 Single-chip Mode

2-1-2 Control Registers

These registers control the bus interface: the memory control register (MEMCTR), the memory moode control register (MEMMDn) and the external memory control register (EXMCTR).

Table 2-1-2 List of Bus Interface Control Registers

Register	Address	R/W	Function
MEMCTR	x'00FC02'	R/W	Memory Control Register
MEMMD0	x'00FC30'	R/W	Memory Mode Control Register 0
MEMMD1	x'00FC32'	R/W	Memory Mode Control Register 1
MEMMD2	x'00FC34'	R/W	Memory Mode Control Register 2
MEMMD3	x'00FC36'	R/W	Memory Mode Control Register 3
EXMCTR	x'00FD00'	R/W	External Memory Control Register

The MEMCTR register and the MEMMDn register need to set the conditions matched the system configuration during the initialization program. [See “9-4 Initialization Program“]

The MEMCTR register sets x’04n0’ (n = 0 to 3, the wait cycle of special registers is normally 1) during the initialization program.

The MEMMD0 register sets the wait cycle for the device connected to Block 0. The bits for selecting bus mode do noe exist in the MEMMD0 register like other MEMMDn registers because the bus width for Block 0 is selected using the pin. Setting the WAIT[1:0] is ignored in the burst ROM support area when using burst ROM.

MEMMD0: x’00FC30’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	WAIT1	WAIT0

Wait cycle for Block 0
00: No wait
01: 1 wait
10: 2 wait
11: Handshake

The MEMMD1 register sets the wait cycles and bus mode for Block 1.

MEMMD1: x'00FC32'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESHT	-	-	-	-	-	-	BSMOD	-	-	-	-	-	-	WAIT1	WAIT0

RE pulse width shortening
0: 1/2 cyc + wait cycle
1: 1/4 cyc + wait cycle

Bus mode for Block 1
0: 16 bit bus mode
1: 8 bit bus mode

Wait cycle for Block 1
00: No wait
01: 1 wait
10: 2 wait
11: Handshake

The MEMMD2 register sets the wait cycles and bus mode for Block 2.

When using the address converted area (x'000000' to x'00DFFF'), set the bus width for block 2 as the same as the bus width for block 0.

MEMMD2: x'00FC34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESHT	—	—	—	—	—	—	BSMOD	—	—	—	—	—	—	WAIT 1	WAIT 0

RE pulse width shortening
0: 1/2 cyc + WAIT cycle
1: 1/4 cyc + WAIT cycle

Wait Cycle Setting for Block 2
00: None
01: 1 cycle
10: 2 cycles
11: Handshake

Bus Width Setting for Block 2
0: 16-bit Bus Width
1: 8-bit Bus Width

The MEMMD3 register sets the wait cycles and bus mode for Block 3.

MEMMD3: x'00FC36'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESHT	—	—	—	—	—	—	BSMOD	—	—	—	—	—	—	WAIT 1	WAIT 0

RE pulse width shortening
0: 1/2 cyc + WAIT cycle
1: 1/4 cyc + WAIT cycle

Wait Cycle Setting for Block 3
00: None
01: 1 cycle
10: 2 cycles
11: Handshake

Bus Width Setting for Block 3
0: 16-bit Bus Width
1: 8-bit Bus Width

The EXMCTR register sets the burst mode for ROM, the polarity of ALE signal during the address/data shared mode, and the pulse width of $\overline{WEH}$ signal and $\overline{WEL}$ signal.

EXMCTR: x'00FD00'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WE SHT	—	—	—	—	—	—	NALE EN	—	—	BRPG 1	BRPG 0	—	—	BREN 1	BREN 0

ROM Burst Mode(*2)
00: Disable
01: Reserved
10: Enable (Without penalty)
11: Enable (With penalty)

Page Size of ROM Burst Mode
00: 4 bytes
01: 8 bytes
10: 16 bytes
11: Reserved

ALE Siganl Polarity
0: Pogitive logic
1: Negative logic
No Wait cycle is forbidden in handshake mode
(address/data separate mode)
0: Disable
1: Enable

WEH, WEL Pulse Width Shortening(*1)
0: Disable
1: Enable

*2 See "2-1-3 ROM Burst Mode Timing" for the penalty availability of burst mode. ROM burst mode without penalty is not allowed during processor mode.

*1 Setting the WESHT bit to 1 makes the rising edge of WEH and WEL 1/4 cycle (25 ns with a 20 MHz oscillator) forward and the hold time of address/data longer.

2-1-3 ROM Burst Mode Timing

This LSI series supports interface for ROM corresponding to burst mode accesses. The burst mode is a mode which reads the data of consecutive few bytes (only few lower bits are changed) at high-speed (access twice faster than normal access).

This series supports the lower 2 bits (4 bytes for page size), the lower 3 bits (8 bytes for page size), and the lower 4 bits (16 bytes for page size).

Use burst mode only during the address/data separated mode. (Do not use burst mode during the address/data shared mode.)
Access area for burst mode is x'080000' to x'0FFFFF'. The access cycle in x'080000' to x'0FFFFF' is 1 wait cycle outside the page and no wait cycle in the page. (Bits[1:0] of the MEMMD0 register are ignored.)

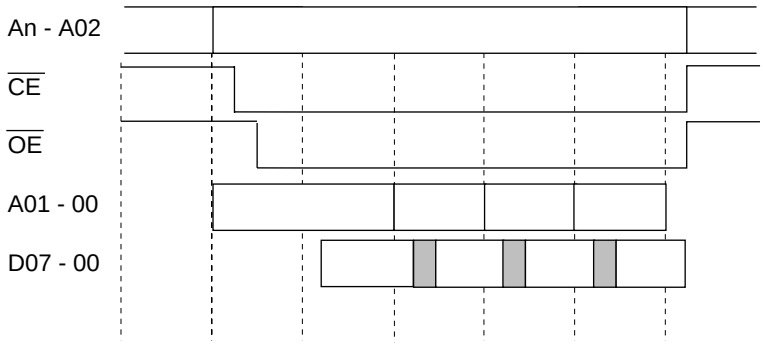
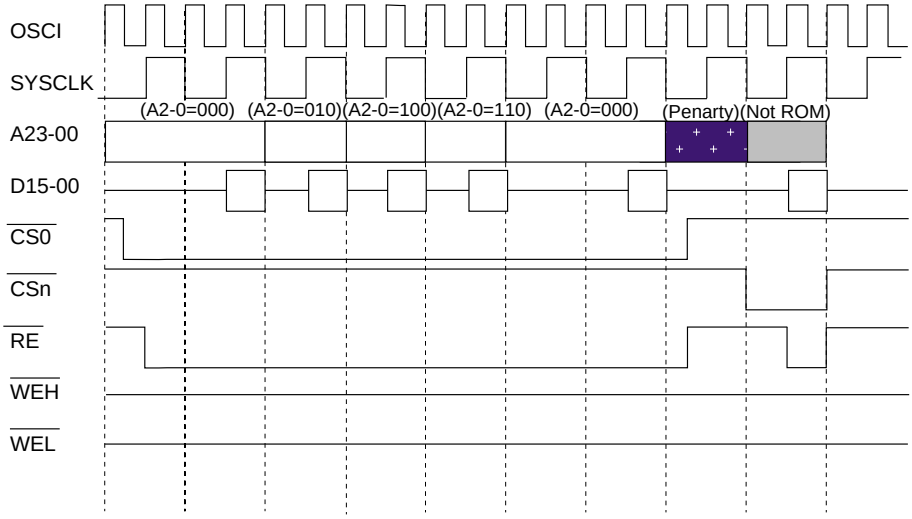


Figure 2-1-8 ROM Timing for Burst Mode (4 bytes for Page Size)

This series has the access cycle with penalty and without penalty when the chip accesses to devices except ROM after it accesses to ROM during the burst mode. Figure 2-1-9 shows their timings and Figure 2-1-10 shows the connection example.

The ROM burst mode is used only during the address/data separated mode and the WAIT pin is ignored even though handshake mode us selected. (Figure 2-1-9 shows the timing of 8 bytes/page during the 16-bit bus mode.)

With Penalty



Without Penalty

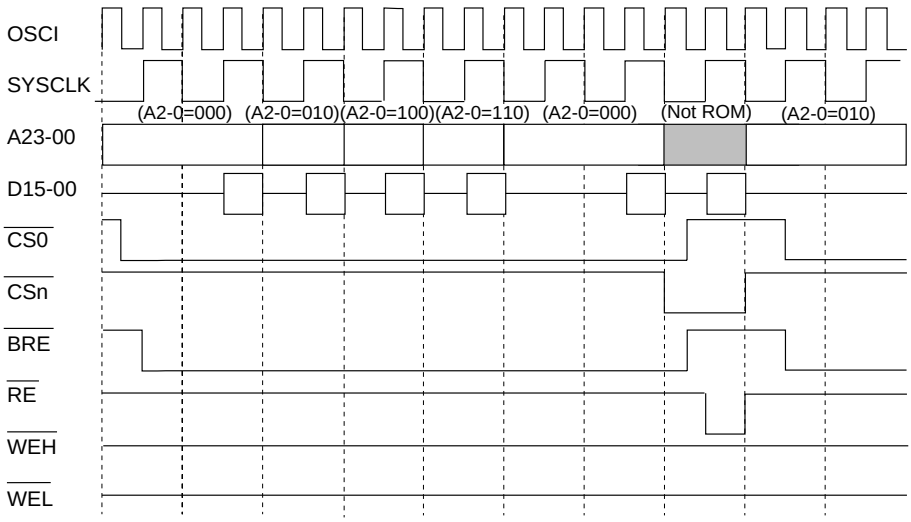


Figure 2-1-9 ROM Burst Mode Access Timing

When the access without penalty is selected, accessing x'010000'Y to x'07FFFF' and x'100000' to x'3FFFFF' is not allowed.

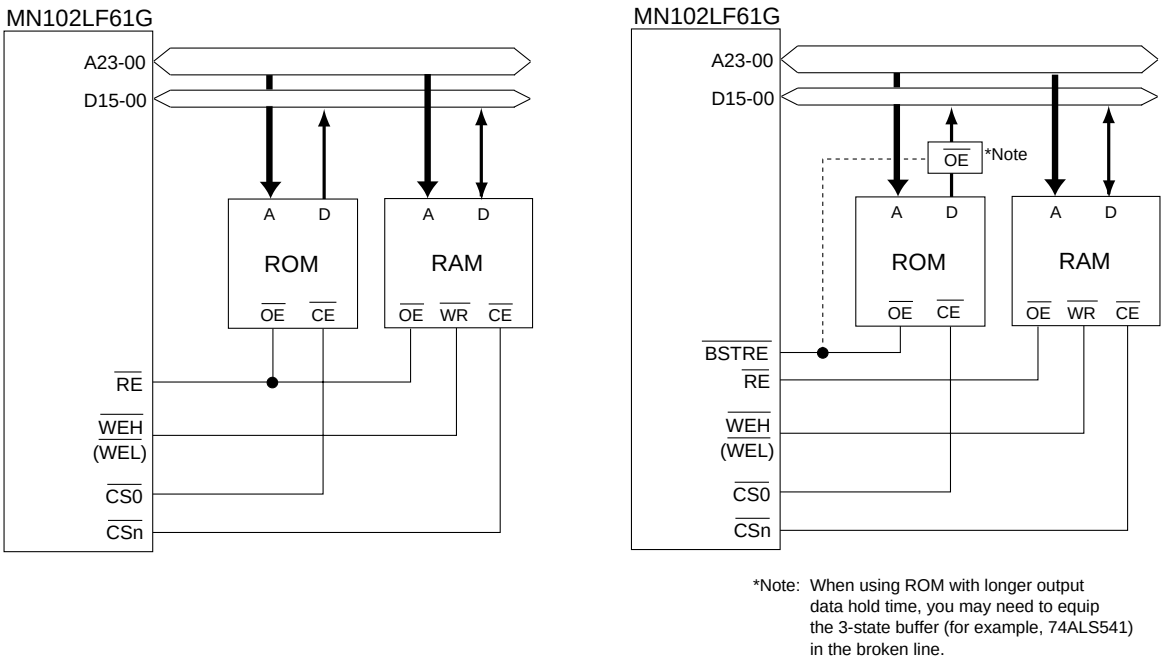


Figure 2-1-10 Access Timing Memory Connection Example During ROM Burst Mode

As Figure 2-1-10 shows, the access is fast but $\overline{RE}$ signal ($\overline{BSTRE}$) for burst ROM is required when access without penalty cycle is selected. In addition, the external 3-state buffer (for example, 74ALS541) may be required when the ROM data hold time is long.

2-2 External Memory Connection Examples

2-2-1 Memory Expansion Mode (Address/Data Separated Mode)

In this LSI series, the control registers for address or data setting need to be set as follows during address/data separated mode. [See Chapter 8 Ports.]

No. 1	Up to 16 bytes (A03 to A00)	8 bit (D15 to D08)	P0DIR= - - - - - - - * P0MD= - - - - - - - * P1DIR= - - - - - - - 0 P1MD= - - - - - - - 1 P2DIR= - - - * - - - 0 P2MD= - - - 0 - - - 1 P3DIR= * * * * * * * * P3MD= 0 0 0 0 0 0 0 0 P4DIR= * * * * * * * * P4MD= 0 0 0 0 0 0 0 0	Use D07 to D00 as general-purpose ports. Use A23 to A04 as general-purpose ports.
		16 bit (D15 to D00)	P0DIR= - - - - - - - 0 P0MD= - - - - - - - 1 P1DIR to P4DIR and P1MD to P4MD are same as those in the above 8-bit bus width of No. 1.	Use A23 to A04 as general-purpose ports.
No. 2	Up to 256 bytes (A07 to A00)	8 bit (D15 to D08)	P0DIR= - - - - - - - * P0MD= - - - - - - - * P1DIR= - - - - - - - 0 P1MD= - - - - - - - 1 P2DIR= - - - 0 - - - 0 P2MD= - - - 1 - - - 1 P3DIR to P4DIR and P1MD to P4MD are same as those in the above 8-bit bus width of No. 1.	Use D07 to D00 as general-purpose ports. Use A23 to A08 as general-purpose ports.
		16 bit (D15 to D00)	P0DIR= - - - - - - - 0 P0MD= - - - - - - - 1 P1DIR to P4DIR and P1MD to P4MD are same as those in the above 8-bit bus width.	Use A23 to A08 as general-purpose ports.
No.3	Up to 512 bytes (A08 to A00)	8 bit (D15 to D08)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 8-bit bus width of No. 1. P3DIR= * * * * * * * 0 P3MD= 0 0 0 0 0 0 0 1	Use D07 to D00 as general-purpose ports. Use A23 to A09 as general-purpose ports.
		16 bit (D15 to D00)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 16-bit bus width of No. 1. P3DIR and P3MD are same as those in the above 8-bit bus width.	Use A23 to A09 as general-purpose ports.
No.4	Up to 1k bytes (A09 to A00)	8bit (D15 to D08)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 8-bit bus width of No. 1. P3DIR= * * * * * * 0 0 P3MD= 0 0 0 0 0 0 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A10 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 16-bit bus width of No. 1. P3DIR and P3MD are same as those in the above 8-bit bus width.	Use A23 to A10 as general-purpose ports.
No.5	Up to 2k bytes (A10 to A00)	8bit (D15 to D08)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 8-bit bus width of No. 1. P3DIR= * * * * * 0 0 0 P3MD= 0 0 0 0 0 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A11 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 16-bit bus width of No. 1. P3DIR and P3MD are same as those in the above 8-bit bus width.	Use A23 to A11 as general-purpose ports.
No.6	Up to 4k bytes (A11 to A00)	8bit (D15 to D08)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 8-bit bus width of No. 1. P3DIR= * * * * 0 0 0 0 P3MD= 0 0 0 0 1 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A12 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 16-bit bus width of No. 1. P3DIR and P3MD are same as those in the above 8-bit bus width.	Use A23 to A12 as general-purpose ports.
No.7	Up to 8k bytes (A12 to A00)	8bit (D15 to D08)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 8-bit bus width of No. 1. P3DIR= * * * 0 0 0 0 0 P3MD= 0 0 0 1 1 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A13 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 16-bit bus width of No. 1. P3DIR and P3MD are same as those in the above 8-bit bus width.	Use A23 to A13 as general-purpose ports.

No.8	Up to 16k bytes (A13 to A00)	8bit (D15 to D08)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 8-bit bus width of No. 1. P3DIR= * * 0 0 0 0 0 0 P3MD= 0 0 1 1 1 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A14 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 16-bit bus width of No. 1. P3DIR and P3MD are same as those in the above 8-bit bus width.	Use A23 to A14 as general-purpose ports.
No.9	Up to 32k bytes (A14 to A00)	8bit (D15 to D08)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 8-bit bus width of No. 1. P3DIR= * 0 0 0 0 0 0 0 P3MD= 0 1 1 1 1 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A15 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 16-bit bus width of No. 1. P3DIR and P3MD are same as those in the above 8-bit bus width.	Use A23 to A15 as general-purpose ports.
No.10	Up to 64k bytes (A15 to A00)	8bit (D15 to D08)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 8-bit bus width of No. 1. P3DIR= 0 0 0 0 0 0 0 0 P3MD= 1 1 1 1 1 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A16 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P2DIR, P4DIR and P0MD to P2MD, P4MD are same as those in the above 16-bit bus width of No. 1. P3DIR and P3MD are same as those in the above 8-bit bus width.	Use A23 to A16 as general-purpose ports.
No.11	Up to 128k bytes (A16 to A00)	8bit (All Spaces) (D15 to D08)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 8-bit bus width of No. 10. P4DIR= * * * * * * * 0 P4MD= 0 0 0 0 0 0 0 1	Use D07 to D00 as general-purpose ports. Use A23 to A17 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 16-bit bus width of No. 10. P4DIR and P4MD are same as those in the above 8-bit bus width.	Use A23 to A17 as general-purpose ports.
No.12	Up to 256k bytes (A17 to A00)	8bit (All Spaces) (D15 to D08)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 8-bit bus width of No. 10. P4DIR= * * * * * * 0 0 P4MD= 0 0 0 0 0 0 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A18 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 16-bit bus width of No. 10. P4DIR and P4MD are same as those in the above 8-bit bus width.	Use A23 to A18 as general-purpose ports.
No.13	Up to 512k bytes (A18 to A00)	8bit (All Spaces) (D15 to D08)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 8-bit bus width of No. 10. P4DIR= * * * * * 0 0 0 P4MD= 0 0 0 0 0 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A19 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 16-bit bus width of No. 10. P4DIR and P4MD are same as those in the above 8-bit bus width.	Use A23 to A19 as general-purpose ports.
No.14	Up to 1M bytes (A18 to A00)	8bit (All Spaces) (D15 to D08)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 8-bit bus width of No. 10. P4DIR= * * * * 0 0 0 0 P4MD= 0 0 0 0 1 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A20 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 16-bit bus width of No. 10. P4DIR and P4MD are same as those in the above 8-bit bus width.	Use A23 to A20 as general-purpose ports.
No.15	Up to 2M bytes (A19 to A00)	8bit (All Spaces) (D15 to D08)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 8-bit bus width of No. 10. P4DIR= * * * 0 0 0 0 0 P4MD= 0 0 0 1 1 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A21 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 16-bit bus width of No. 10. P4DIR and P4MD are same as those in the above 8-bit bus width.	Use A23 to A21 as general-purpose ports.
No.16	Up to 4M bytes (A20 to A00)	8bit (All Spaces) (D15 to D08)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 8-bit bus width of No. 10. P4DIR= * * 0 0 0 0 0 0 P4MD= 0 0 1 1 1 1 1 1	Use D07 to D00 as general-purpose ports. Use A23 to A22 as general-purpose ports.
		16bit (D15 to D00)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 16-bit bus width of No. 10. P4DIR and P4MD are same as those in the above 8-bit bus width.	Use A23 to A22 as general-purpose ports.
No.17	Up to 8M bytes (A21 to A00) Or (/CS2 to /CS0, A21 to A00)	8bit (All Spaces) (D15 to D08)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 8-bit bus width of No. 10. P4DIR= * 0 0 0 0 0 0 0 P4MD= 0 1 1 1 1 1 1 1 P6MD= * 0 - - * * * -	Use D07 to D00 as general-purpose ports. In addition, use A22 as a general-purpose port when the address is determined by /CS2 to /CS0.
		16bit (D15 to D00)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 16-bit bus width of No. 10. P4DIR and P4MD are same as those in the above 8-bit bus width.	Use A23 as a general-purpose port. In addition, use A22 as a general-purpose port when the address is determined by /CS2 to /CS0.
No.18	Up to 16M bytes (A23 to A00) Or (/CS3 to /CS0, A23 to A00)	8bit (All Spaces) (D15 to D08)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 8-bit bus width of No. 10. P4DIR= 0 0 0 0 0 0 0 0 P4MD= 1 1 1 1 1 1 1 1 P6MD= 0 0 - - * * * -	Use D07 to D00 as general-purpose ports. In addition, use A23 to A22 as general-purpose ports when the address is determined by /CS3 to CS0.
		16bit (D15 to D00)	P0DIR to P3DIR and P0MD to P3MD are same as those in the above 16-bit bus width of No. 10. P4DIR and P4MD are same as those in the above 8-bit bus width.	Use /CS3 to /CS0 as general-purpose ports. In addition, use A23 to A22 as general-purpose ports when the address is determined by /CS3 to CS0.

2-2-2 External Memory Connection Examples (Address/Data Separeted Mode)

This section describes the external memory connection examples.

■ Memory System with 16-bit Bus Width

The following is the example of connecting the 4-Mbit ROM (256 kilowords × 16 bits), the 1-Mbit SRAM (128 kilo words × 8 bits) and the ASIC with 16-bit bus width to the $\overline{CS0}$ area (1 wait cycle fixed), the $\overline{CS1}$ area (no wait cycle fixed) and the $\overline{CS3}$ area (handshake), respectively.

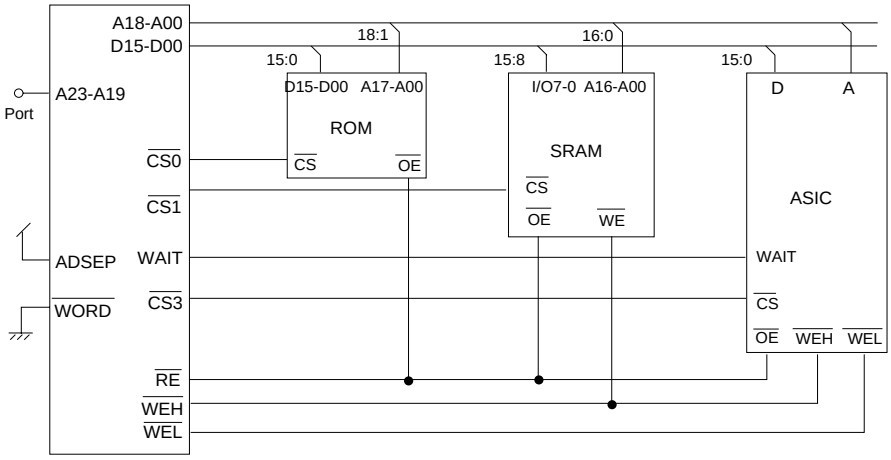


Figure 2-2-1 Memory Connection Example with 16-bit Bus Width (Address/Data Separated Mode)

MEMMD0: x'00FC30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	1

MEMMD1: x'00FC32'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	1	-	-	-	-	-	-	0	0

MEMMD3: x'00FC36'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	0	-	-	-	-	-	-	1	1

■ Memory System with 8-bit Bus Width in All Areas

The following is the example of connecting the 4-Mbit ROM (512 kilowords × 8 bits), the 1-Mbit SRAM (128 kilowords × 8 bits) and the ASIC with 8-bit bus width to the $\overline{CS0}$ area (2 wait cycles fixed), the $\overline{CS1}$ area (1 wait cycle fixed) and the $\overline{CS3}$ area (handshake), respectively.

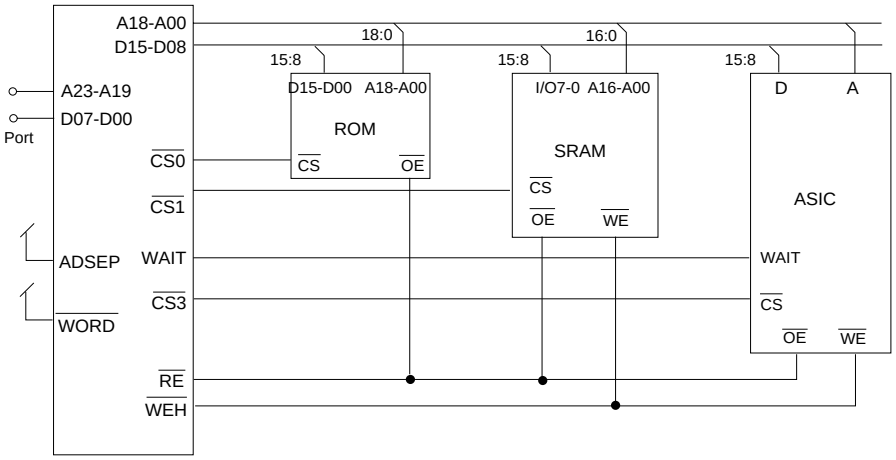


Figure 2-2-2 Memory Connection Example with 8-bit Bus Width (Address/Data Separated Mode)

MEMMD0: x'00FC30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	0

In the MN102L series, the data is input to the upper pins of D15 to D08.

MEMMD1: x'00FC32'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	1	-	-	-	-	-	-	0	1

MEMMD3: x'00FC36'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	1	-	-	-	-	-	-	1	1

■ ROM, RAM Access Timing with 16-bit Bus Width

Dotted lines, $\overline{WEH}$ and $\overline{WEL}$ show waveforms when WE width shortening (EXMCTR) bit15 is set.

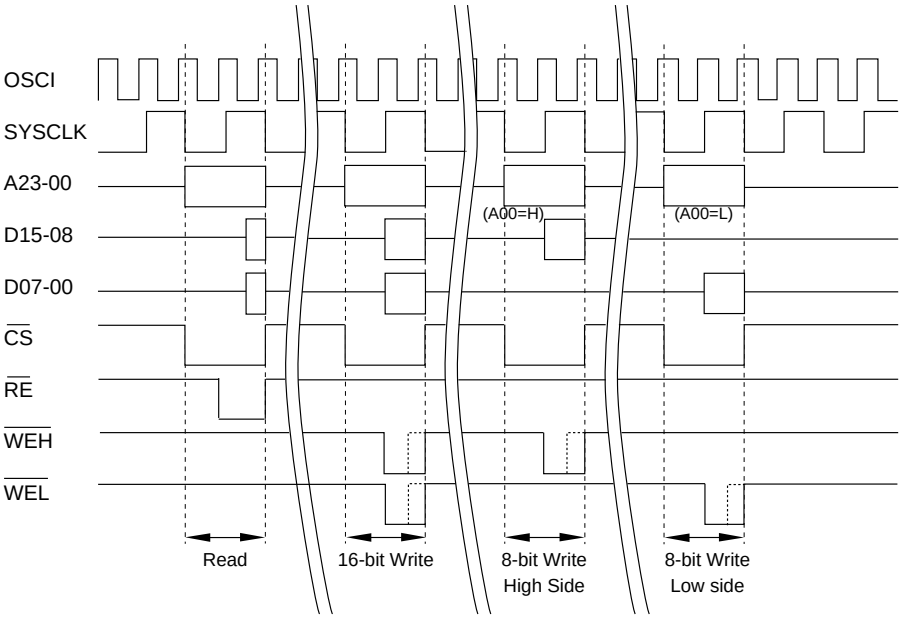


Figure 2-2-3 No Wait Access Timing with 16-bit Bus Width

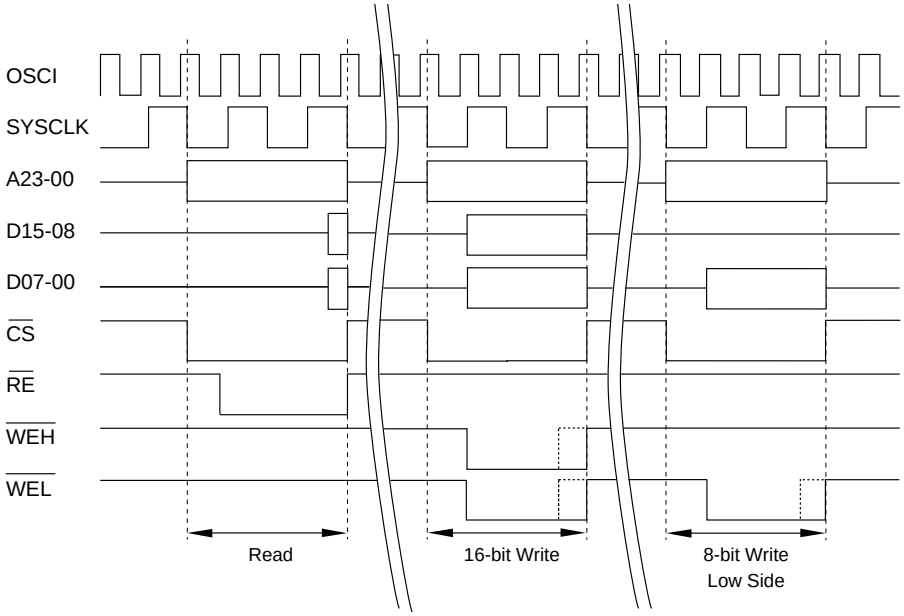


Figure 2-2-4 1 Wait Access Timing with 16-bit Bus Width

■ ROM, RAM Access Timing with 16-bit Bus Width

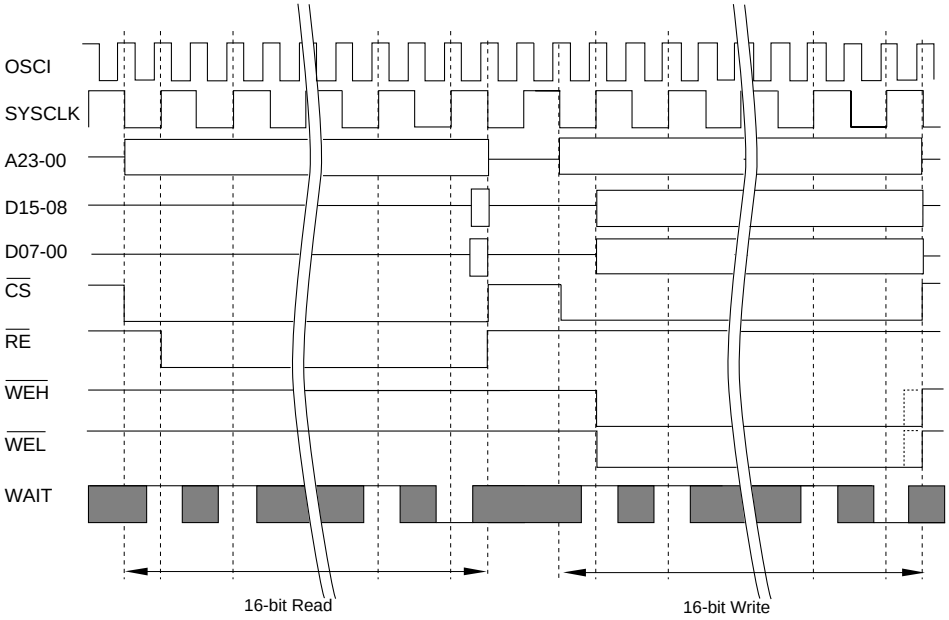


Figure 2-2-5 Handshake Access Timing with 16-bit Bus Width

■ ROM, RAM Access Timing with 8-bit Bus Width

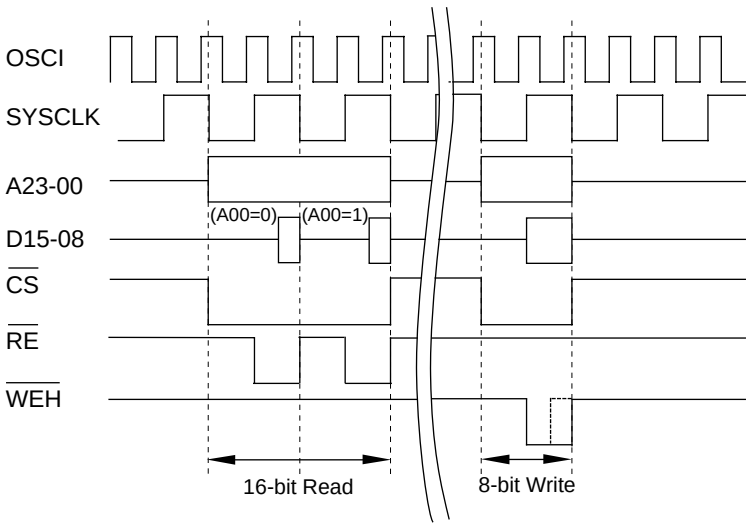


Figure 2-2-6 No Wait Access Timing with 8-bit Bus Width

■ ROM, RAM Access Timing with 8-bit Bus Width

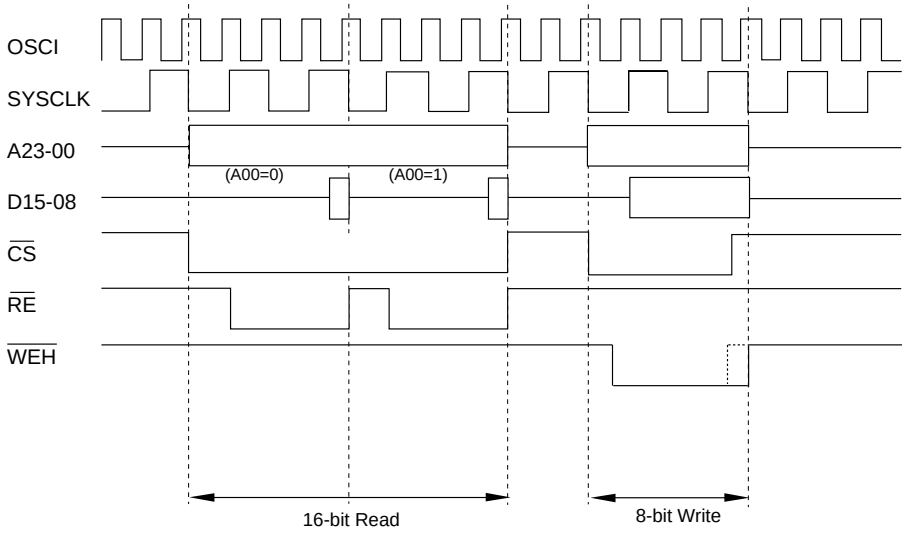


Figure 2-2-7 1 Wait Access Timing with 8-bit Bus Width

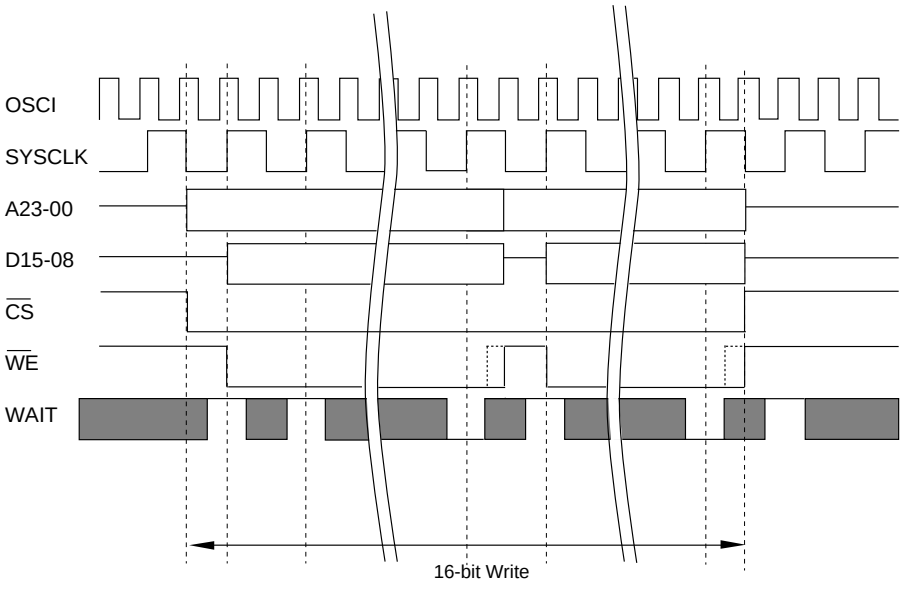


Figure 2-2-8 Handshake Access Timing with 8-bit Bus Width

■ Access Timing during Bus Request (Address/Data Separated Mode)

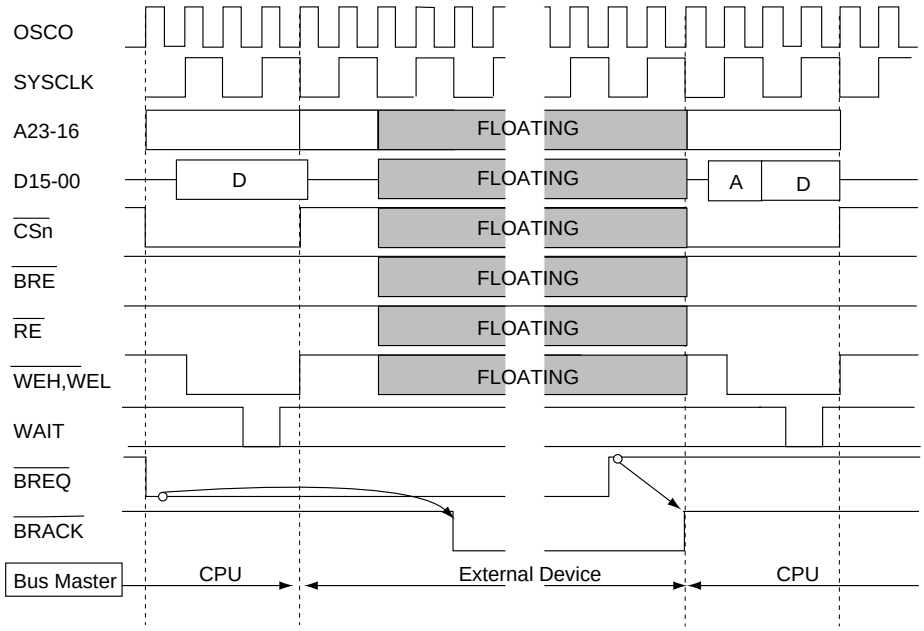


Figure 2-2-9 Access Timing during Bus Request (Address/Data Separated Mode)

2-2-3 Memory Expansion Mode (Address/Data Shared Mode)

In this LSI series, the control registers for address or data setting need to be set as follows during address/data shared mode. [See Chapter 8 Ports.]

No.1	Up to 64 Kbytes	8/16bit	P0DIR=[-][-][-][-][-][-][-][0] P0MD=[-][-][-][-][-][-][-][1] P1DIR=[-][-][-][-][-][-][-][0] P1MD=[-][-][-][-][-][-][-][1] P4DIR=[*][*][*][*][*][*][*][0] P4MD=[0][0][0][0][0][0][0][0]	Use A23 to A16 as general-purpose ports.
No.2	Up to 128 Kbytes	8/16bit	P0DIR to P1DIR and P0MD and P1MD are set as same as those in the above. P4DIR=[*][*][*][*][*][*][*][1] P4MD=[0][0][0][0][0][0][0][1]	Use A23 to A17 as general-purpose ports.
No.3	Up to 256 Kbytes	8/16bit	P0DIR to P1DIR and P0MD and P1MD are set as same as those in the above. P4DIR=[*][*][*][*][*][*][1][1] P4MD=[0][0][0][0][0][0][1][1]	Use A23 to A18 as general-purpose ports.
No.4	Up to 512 Kbytes	8/16bit	P0DIR to P1DIR and P0MD and P1MD are set as same as those in the above. P4DIR=[*][*][*][*][*][1][1][1] P4MD=[0][0][0][0][0][1][1][1]	Use A23 to A19 as general-purpose ports.
No.5	Up to 1 Mbyte	8/16bit	P0DIR to P1DIR and P0MD and P1MD are set as same as those in the above. P4DIR=[*][*][*][*][1][1][1][1] P4MD=[0][0][0][0][1][1][1][1]	Use A23 to A20 as general-purpose ports.
No.6	Up to 2 Mbytes	8/16bit	P0DIR to P1DIR and P0MD and P1MD are set as same as those in the above. P4DIR=[*][*][*][1][1][1][1][1] P4MD=[0][0][0][1][1][1][1][1]	Use A23 to A21 as general-purpose ports.
No.7	Up to 4 Mbytes	8/16bit	P0DIR to P1DIR and P0MD and P1MD are set as same as those in the above. P4DIR=[*][*][1][1][1][1][1][1] P4MD=[0][0][1][1][1][1][1][1]	Use A23 to A22 as general-purpose ports.
No.8	Up to 8 Mbytes	8/16bit	P0DIR to P1DIR and P0MD and P1MD are set as same as those in the above. P4DIR=[*][1][1][1][1][1][1][1] P4MD=[0][1][1][1][1][1][1][1] P6MD=[*][0][-][-][*][*][*][-]	Use A23 as a general-purpose port.
No.9	Up to 16 Mbytes	8/16bit	P0DIR to P1DIR and P0MD and P1MD are set as same as those in the above. P4DIR=[1][1][1][1][1][1][1][1] P4MD=[1][1][1][1][1][1][1][1] P6MD=[0][0][-][-][*][*][*][-]	

2-2-4 External Memory Connection Examples (Address/Data Shared Mode)

This section describes the external memory connection examples.

■ Memory System with 16-bit Bus Width

The following is the example of connecting the 4-Mbit ROM (256 kilo words × 16 bits), the 1-Mbit SRAM (128 kilo words × 8 bits) and the ASIC with 16-bit bus width to the $\overline{CS0}$ area (1 wait cycle fixed), the $\overline{CS1}$ area (1 wait cycle fixed) and the $\overline{CS3}$ area (handshake), respectively.

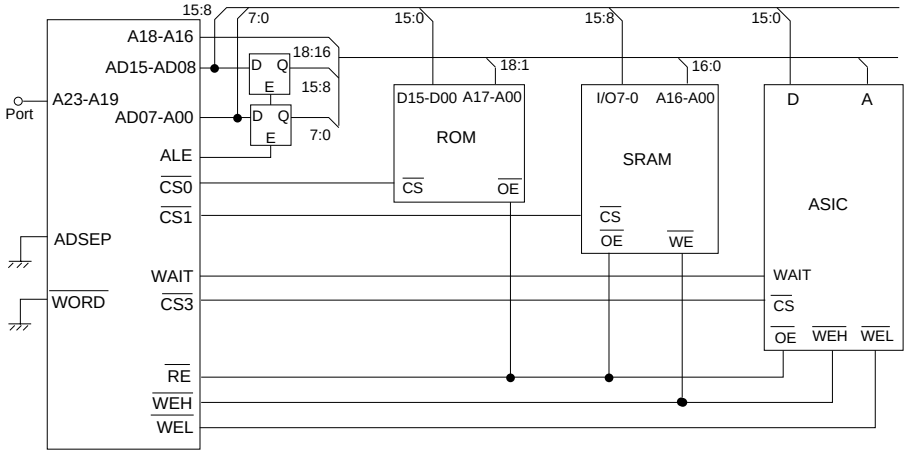


Figure 2-2-10 Memory Connection Example with 16-bit Bus Width (Address/Data Shared Mode)

During the address/data shared mode, this LSI series operates in 1 wait cycle even though WAIT[1:0] are set to '00'.

MEMMD0: x'00FC30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	1

MEMMD1: x'00FC32'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	1	-	-	-	-	-	-	0	1

MEMMD3: x'00FC36'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	0	-	-	-	-	-	-	1	1

■ Memory System with 8-bit Bus Width in All Areas

The following is the example of connecting the 4-Mbit ROM (512 kilo words × 8 bits), the 1-Mbit SRAM (128 kilo words × 8 bits) and the ASIC with 8-bit bus width to the $\overline{CS0}$ area (2 wait cycles fixed), the $\overline{CS1}$ area (1 wait cycle fixed) and the $\overline{CS3}$ area (handshake), respectively.

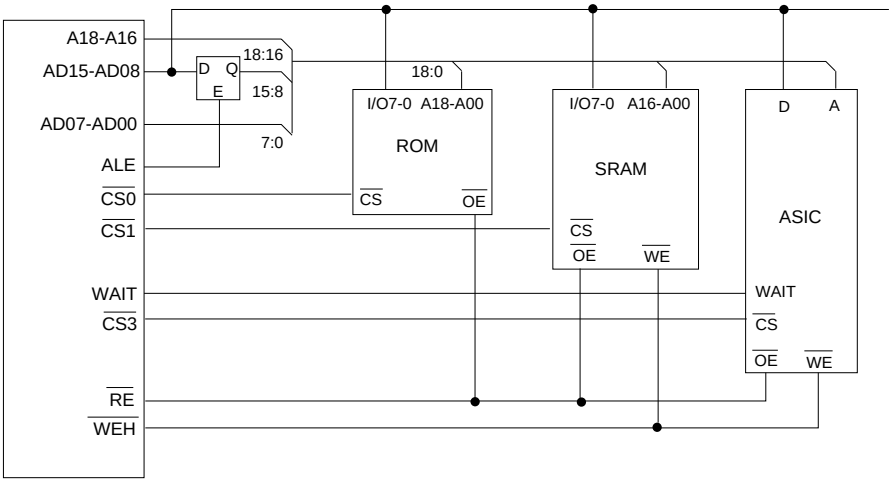


Figure 2-2-11 Memory Connection Example with 8-bit Bus Width (Address/Data Shared Mode)

MEMMD0: x'00FC30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	0

MEMMD1: x'00FC32'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	1	-	-	-	-	-	-	0	1

MEMMD3: x'00FC36'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT1	WAIT0
-	-	-	-	-	-	-	1	-	-	-	-	-	-	1	1

In the MN102 series, the data is input to the upper pins of D15 to D08.

■ ROM, RAM Access Timing with 16-bit Bus Width

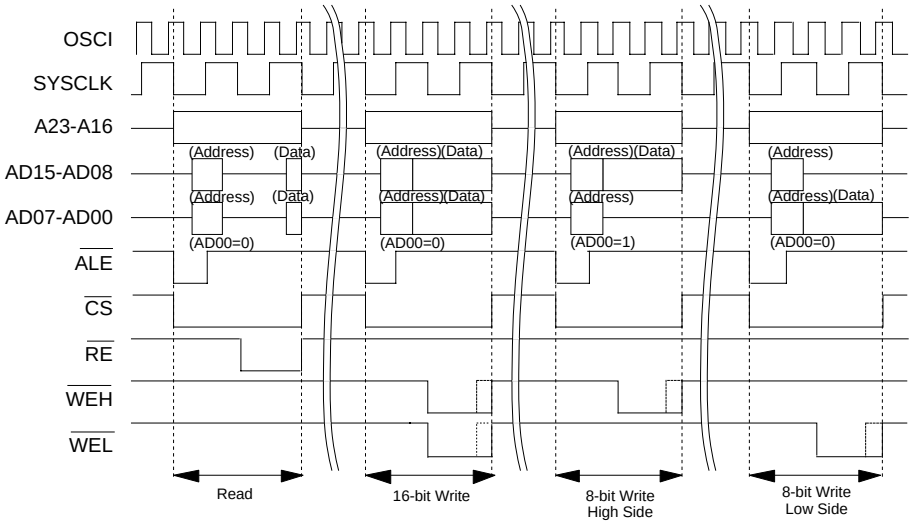


Figure 2-2-12 Fixed Wait Access Timing with 16-bit Bus Width

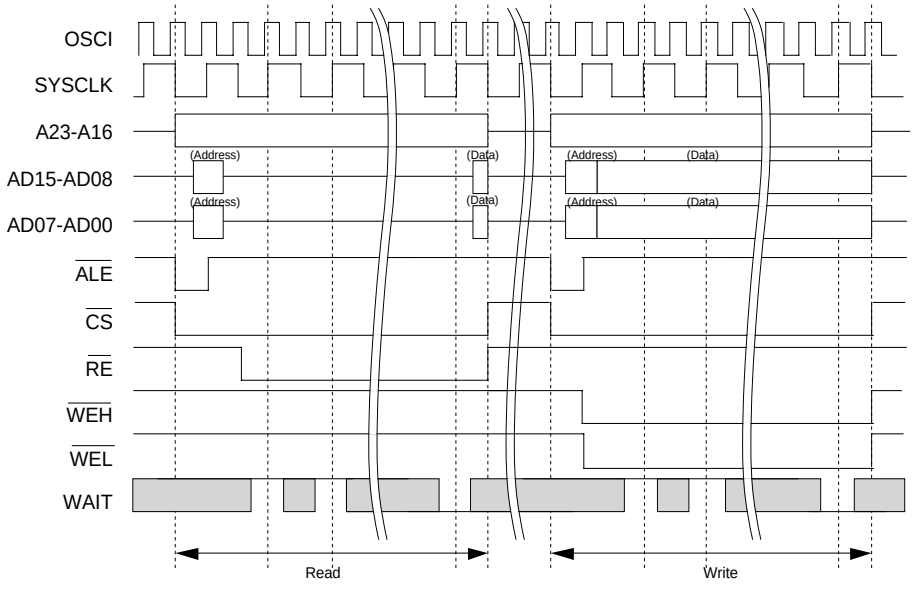


Figure 2-2-13 Handshake Access Timing with 16-bit Bus Width

■ ROM, RAM Access Timing with 8-bit Bus Width

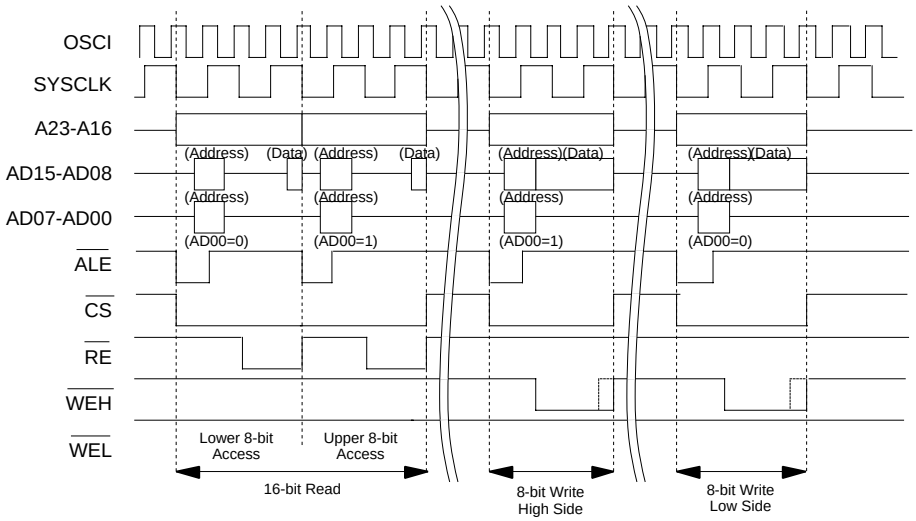


Figure 2-2-14 Fixed Wait Access Timing with 8-bit Bus Width

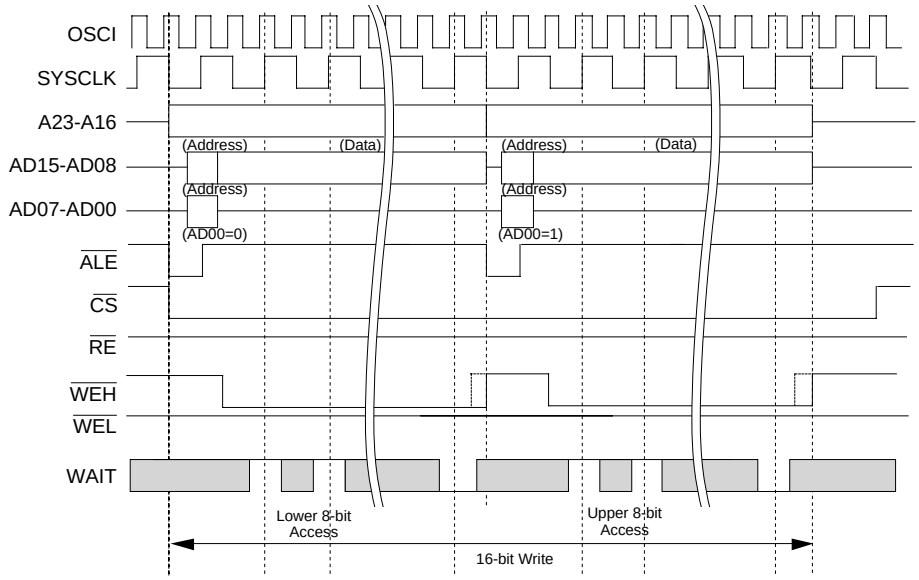


Figure 2-2-15 Handshake Access Timing with 8-bit Bus Width

■ Access Timing during Bus Request (Address/Data Shared Mode)

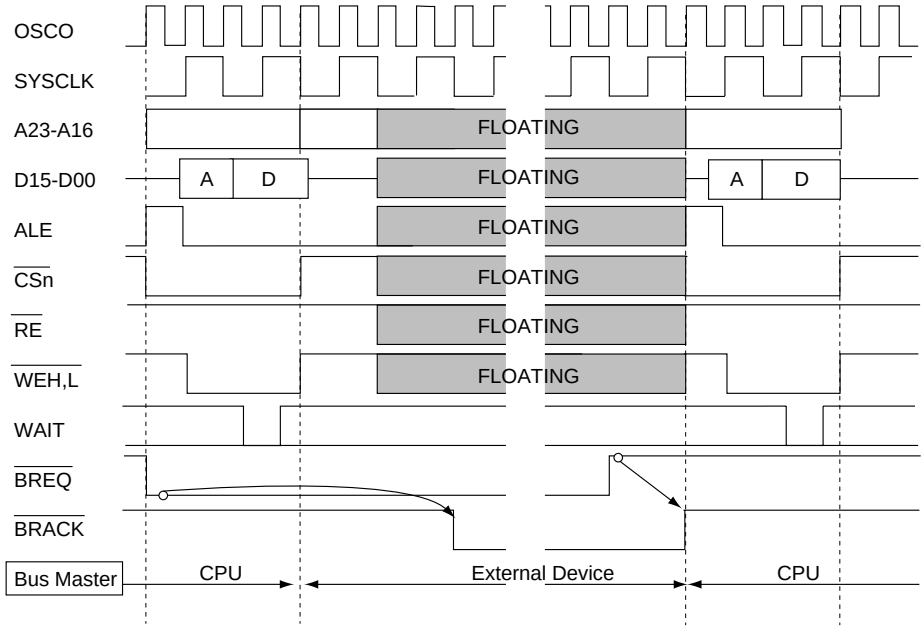


Figure 2-2-16 Access Timing during Bus Request (Address/Data Shared Mode)

Chapter 3 Interrupts

3

3-1 Interrupt Groups

3-1-1 Overview

The interrupt controller contains eight groups. Each group has some interrupt vectors . When an interrupt occurs, the CPU receives an interrupt request. [☞MN102L Series LSI User's Manual]

Table 3-1-1 List of Interrupt Control Registers

Interrupt Group	Interrupt Vector (Number is IDTn bit position)	Control Register
Group 0	2 Undefined Instruction Interrupt 1 Watchdog Timer Interrupt 0 NMI Interrupt	Non-maskable Interrupt Control Register 0 G0ICR: x'00FC40'
Group 1	3 Reserved 2 Timer/Counter 5 Underflow 1 Timer/Counter 0 Underflow 0 External Interrupt IRQ0	Maskable Interrupt Control Register 1 G1ICR: x'00FC42'
Group 2	3 Reserved 2 A/D Conversion End 1 Timer/Counter 1 Underflow 0 External Interrupt IRQ1	Maskable Interrupt Control Register 2 G2ICR: x'00FC44'
Group 3	3 Serial Ch0 Reception End 2 Serial Ch0 Transmission End 1 Timer/Counter 2 Underflow 0 External Interrupt IRQ2	Maskable Interrupt Control Register 3 G3ICR: x'00FC46'
Group 4	3 Serial Ch1 Reception End 2 Serial Ch1 Transmission End 1 Timer/Counter 3 Underflow 0 External Interrupt IRQ3	Maskable Interrupt Control Register 4 G4ICR: x'00FC48'
Group 5	3 Reserved (Set the corresponding enable flag always to 0.) 2 Reserved (Set the corresponding enable flag always to 0.) 1 Timer/Counter 4 Underflow 0 External Interrupt IRQ4	Maskable Interrupt Control Register 5 G5ICR: x'00FC4A'
Group 6	3 ATC Completion 2 Timer/Counter 6 Compare Capture B 1 Timer/Counter 6 Compare Capture A 0 Timer/Counter 6 Underflow	Maskable Interrupt Control Register 6 G6ICR: x'00FC4C'
Group 7	3 Reserved 2 Timer/Counter 7 Compare Capture B 1 Timer/Counter 7 Compare Capture A 0 Timer/Counter 7 Underflow	Maskable Interrupt Control Register 7 G7ICR: x'00FC4E'

Reserved: A corresponding flag does not actually exist.

The control registers are assigned to each corresponding interrupt group except Group 0 and control the assigned interrupt vectors. For example, in the MN102LF 53G, when timer 0 becomes underflow, the interrupt request flag (IRF1=TM0IR) of the maskable interrupt control register 1 (G1ICR) becomes 1. At this point, an interrupt request is output to the CPU core if the corresponding interrupt enable flag (IEN1=TM0IE) is 1. Comparing the interrupt mask level (IM2 to 0) of the processor status word (PSW) with the group interrupt level (ILVn=G1LV[2:0]) of the G1ICR register and the interrupt enable flag (IE) of PSW determine whether the CPU core receives the interrupt or not.

G1ICR: x'00FC42'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	G1 LV2	G1 LV1	G1 LV0	—	TM5 IE	TM0 IE	IRQ0 IE	—	TM5 IR	TM0 IR	IRQ0 IR	—	TM5 ID	TM0 ID	IRQ0 ID

Group interrupt level
ILVn
Setup of interrupt level

Interrupt enable flag
IENn
Setup of interrupt permission

Interrupt demand flag
IRFn
Occurrence of interrupt factor

Interrupt detective flag
IDTn
Detection of interrupt demand

Please refer to "2-5 Interrupt Controller" in the MN102L Series LSI User's Manual for detail operations, and the MN102L Series Instruction Manual for interrupt handling flow and handler programming.

Set the interrupt enable flags IEN [3:2] (bits [11:10]) of the G7ICR always to 0.

3-2 External Interrupts

3-2-1 External Pin Interrupts

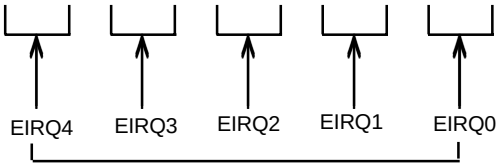
Group 1 to Group 5 control external pin interrupts.

The EXTMD register sets the interrupt conditions.

The EXTMD register sets the interrupt levels and timing of external interrupts, and specifies each pins' level or edge.

EXTMD: x'00FC56'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	IRQ4 TG1	IRQ4 TG0	IRQ3 TG1	IRQ3 TG0	IRQ2 TG1	IRQ2 TG0	IRQ1 TG1	IRQ1 TG0	IRQ0 TG1	IRQ0 TG0



00: An interrupt occurs at low level.
01: An interrupt occurs at high level.
10: An interrupt occurs at negative edge.
11: An interrupt occurs at positive edge.

3-2-2 NMI Pin Interrupts

This series supports an NMI interrupt. The $\overline{\text{NMI}}$ interrupt occurs on the negative edge of NMI pin.

NMI does not occur when microcontroller is in bus release status.

3-3 Interrupt Setup Examples

3-3-1 External Pin Interrupt Setup

An interrupt occurs on the negative (falling) edge from the external interrupt pin IRQ0 (PA0).

The external interrupt edge specification register (EXTMD) is set to the interrupt request generation at low level after reset release, and the IRQ0IR bit of the maskable interrupt control register 1 (G1ICR) becomes 0.

■ Interrupt Enable Setup

(1) Set the interrupt conditions of the interrupt pin IRQ0 (PA0). In this case, set the IRQ0TG of the EXTMD register to 2 (bit string 10:negative edge).

EXTMD: x'00FC50'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	IRQ4 TG1	IRQ4 TG0	IRQ3 TG1	IRQ3 TG0	IRQ2 TG1	IRQ2 TG0	IRQ1 TG1	IRQ1 TG0	IRQ0 TG1	IRQ0 TG0
-	-	-	-	-	-	0	0	0	0	0	0	0	0	1	0

In this example, the interrupt level is 4.

(2) Enable interrupts. At this point, clear all prior interrupt requests. To do this, set G1LV[2:0], IRQ0IR and IRQ0IE of the maskable interrupt control register 1 (G1ICR) to an interrupt level, 0 and 1, respectively.

G1ICR: x'00FC42'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	G1 LV2	G1 LV1	G1 LV0	—	TM5 IE	TM0 IE	IRQ0 IE	—	TM5 IR	TM0 IR	IRQ0 IR	—	TM5 ID	TM0 ID	IRQ0 ID
-	1	0	0	-	0	0	1	-	0	0	0	-	0	0	0

(3) Enable interrupts by setting the interrupt enable flag (IE) of the processor status Word (PSW) to 1 and the interrupt mask level (IMn) to 7 (bit string 111).

Thereafter, an interrupt occurs when the negative (falling) edge is generated on the interrupt pin IRQ0 (PA0). The program branches to x'080008' when the interrupt is accepted.

■ Interrupt Handling

(4) Specify the interrupt group by reading the interrupt accept group register (IAGR) during interrupt prehandling.

Normally, the program generates the interrupt start address and branches to that address.

(5) Specify the interrupt vector in the group by reading the G1ICR register. Check the IRQ0ID with the bit test instruction (BTST). If IRQ0ID is 1, execute the interrupt handling.

During interrupt service routine, the IM and IE of PSW become the interrupt level and 0 respectively. The multiple interrupts are not allowed. It means that other interrupts except the non-maskable interrupt are not accepted during interrupt service routine unless the PSW is set.

(6) Clear the IRQ0IR bit of the G1ICR register.

(7) Return to the main program with the interrupt return instruction (RTI) after the interrupt handling ends.

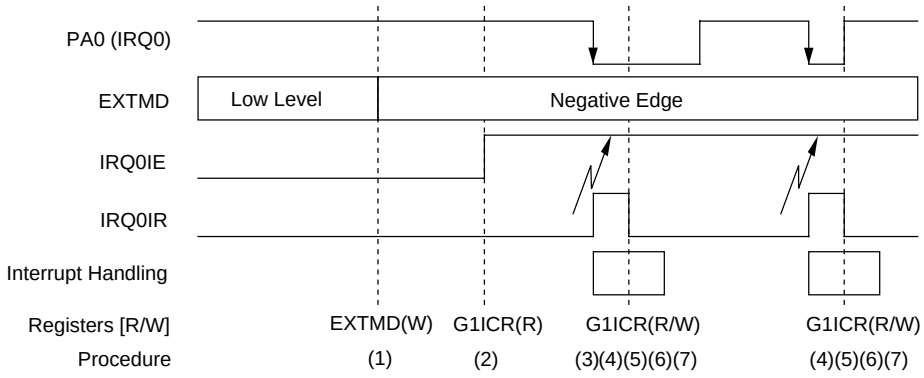


Figure 3-3-1 External Pin Interrupt Timing

3-3-2 Watchdog Timer Interrupt

An interrupt occurs by using the watchdog timer.

When the watchdog fanction is used, operation is started by setting the WDRST flag of the CPU mode control register (CPUM) to enable (‘0’) after reset. The watchdog timer needs to be cleared during the main program because a non-maskable interrupt occurs when the watchdog counter overflows.

■ Interrupt Enable Setup

When the watchdog timer counts 65536 cycles of SYSCLK (6.5536 ms with a 20 MHz oscillator), a watchdog interrupt occurs.

(1) Enable interrupts by setting the interrupt enable flag (IE) of the processor status Word (PSW) to 1 and the interrupt mask level (IMn) to 7 (bit string 111).

(2) Clear the WDRST flag of the CPUM register. This starts the watchdog timer.

CPUM: x’00FC00’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD RST	—	—	—	—	—	—	—	—	—	—	OSC ID	STOP	HALT	OSC1	OSC2
0	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0

■ Watchdog Timer Clear

Normally, clear the watchdog timer before an interrupt occurs.

(3) Set the WDRST flag of the CPUM register to 1 and then immediately clear to 0. The watchdog timer is cleared to 0 when the WDRST flag is 1.

■ Interrupt Handling

Normally, the program generates the interrupt start address and branches to that address.

The program branches to x’080008’ when an interrupt is generated and accepted.

(4) Specify the interrupt group by reading the interrupt accept group register (IAGR) during interrupt prehandling.

The IM of PSW becomes the highest level during interrupt handling and other interrupts are not accepted.

(5) Verify a watchdog interrupt by reading the nonmaskable interrupt control register (G0ICR). Check the WDIF with the bit test instruction (BTST). If WDIF is 1, execute the interrupt service routine.

(6) Clear the WDIF flag of the G0ICR register.

(7) Return to the main program with the interrupt return instruction (RTI) after the interrupt handling ends.

The watchdog timer and the oscillation stabilization wait counter are shared. The watchdog timer operates as the oscillation stabilization wait counter when the CPU returns from the STOP mode. Because of this, the WDIF flag is cleared to 0 when the CPU moves to the STOP mode. The WDIF flag is cleared to 0 again after the CPU moves to the normal mode. [☞ "2-6 Standby Function" in the MN102L Series LSI User's Manual]

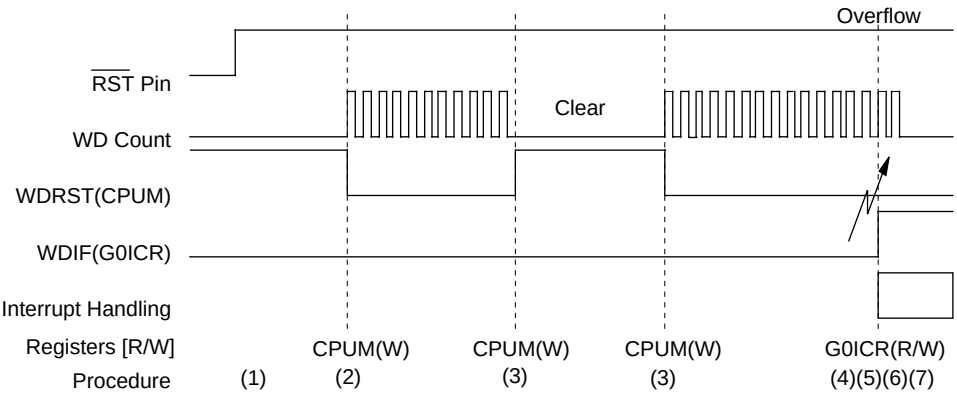


Figure 3-3-2 Watchdog Timer Interrupt Timing

Chapter 4 Timers/Counters

4

4-1 Timers

4-1-1 Overview

This LSI series contains six 8-bit timers (timer 0 to timer 5) and two 16-bit timers (timer 6 and timer 7).

Table 4-1-1 Timer Function (1/2)

Function \ Timer	8-bit Timer			
	Timer 0	Timer 1	Timer 2	Timer 3
Interrupt Request Destination	Group 1 (G1ICR) ・TM0IR	Group 2 (G2ICR) ・TM1IR	Group 3 (G3ICR) ・TM2IR	Group 4 (G4ICR) ・TM3IR
Interrupt Source	Timer 0 underflow	Timer 1 underflow	Timer 2 underflow	Timer 3 underflow
Clock Source	・TM0IO pin ・ ϕ/128(*1) ・ ϕ(*2) ・ fxi/4(*3)	・TM1IO pin ・ fxi/4 ・ Timer 0 ・ ϕ	・TM2IO pin ・ Timer 1 ・ Timer 0 ・ ϕ	・TM3IO pin ・ Timer 2 ・ Timer 0 ・ ϕ
Counting Method	Down counting	Down counting	Down counting	Down counting
Interval Timer	○	○	○	○
Event Counter	○	○	○	○
Timer Output	○	○	○	○
PWM	-	-	-	-
Two-phase Timer Output	-	-	-	-
One-shot Pulse Output	-	-	-	-
One-phase Capture Input	-	-	-	-
Two-phase Capture Input	-	-	-	-
Two-phase Encoder	-	-	-	-
External Count Direction Control	-	-	-	-
External Count Reset Control	-	-	-	-
Serial Interface Transfer Clock Generation	-	-	○	○
A/D Conversion Timing Generation	-	○	-	-

Table 4-1-1 Timer Function (2/2)

Function \ Timer	8-bit Timer		16-bit Timer	
	Timer 4	Timer 5	Timer 6	Timer 7
Interrupt Request Destination	Group 5 (G5ICR) ・TM4IR	Group 1 (G1ICR) ・TM5IR	Group 6 (G6ICR) ・TM6UIR ・TM6AIR ・TM6BIR	Group 7 (G7ICR) ・TM7UIR ・TM7AIR ・TM7BIR
Interrupt Source	Timer 4 underflow	Timer 5 underflow	・Timer 6 underflow ・Timer 6 compare A or capture A match ・Timer 6 compare B or capture B match	・Timer 7 underflow ・Timer 7 compare A or capture A match ・Timer 7 compare B or capture B match
Clock Source	・TM4IO pin ・Timer 3 ・Timer 0 ・fxi/4	・TM5IO pin ・Timer 4 ・Timer 0 ・fxi/4	・SYSCLK ・Timer 4 ・Timer 5 ・TM6IOB pin ・Two-phase encoder	・SYSCLK ・Timer 4 ・Timer 5 ・TM7IOB pin ・Two-phase encoder
Counting Method	Down counting	Down counting	Up/Down counting	Up/Down counting
Interval Timer	○	○	○	○
Event Counter	○	○	○	○
Timer Output	○	○	○	○
PWM	-	-	Arbitrary duty	Arbitrary duty
Two-phase Timer Output	-	-	○	○
One-shot Pulse Output	-	-	○	○
One-phase Capture Input	-	-	○	○
Two-phase Capture Input	-	-	○	○
Two-phase Encoder	-	-	4x, 1x	4x, 1x
External Count Direction Control	-	-	○	○
External Count Reset Control	-	-	○	○
Serial Interface Transfer Clock Generation	-	-	-	-
A/D Conversion Timing Generation	-	-	-	-

*1 System Clock (10 MHz with a 20-MHz ocillator)/128
*2 System Clock (10 MHz with a 20-MHz ocillator)
*3 Low-speed Clock (32 kHz)/4

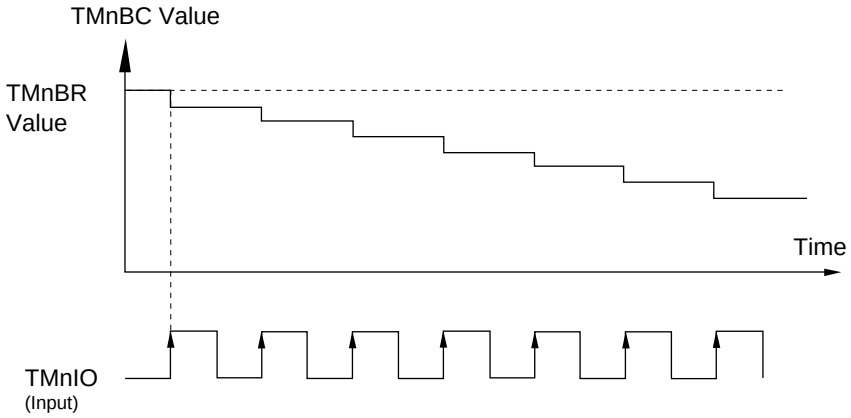


Figure 4-1-1 Event Counter Timing (Timer 0 to Timer 5)

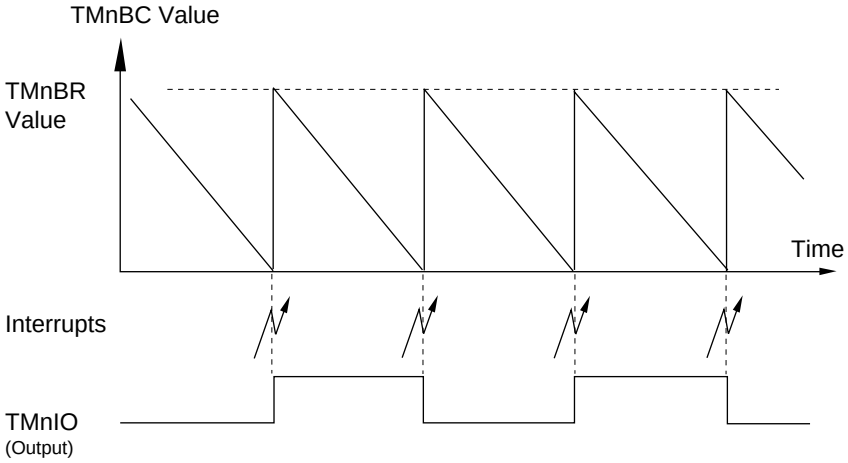


Figure 4-1-2 Timer Output, Interval Timer Timing (Timer 0 to Timer 5)

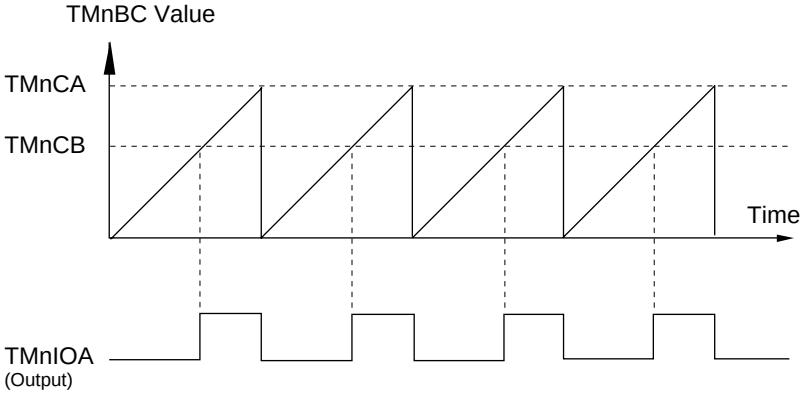


Figure 4-1-3 PWM Output Timing (Timer 6 and Timer 7)

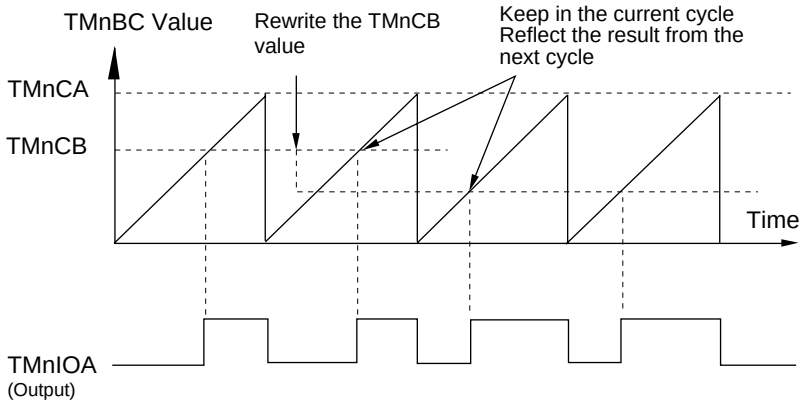


Figure 4-1-4 PWM Output Timing (Data Write) (Timer 6 and Timer 7)

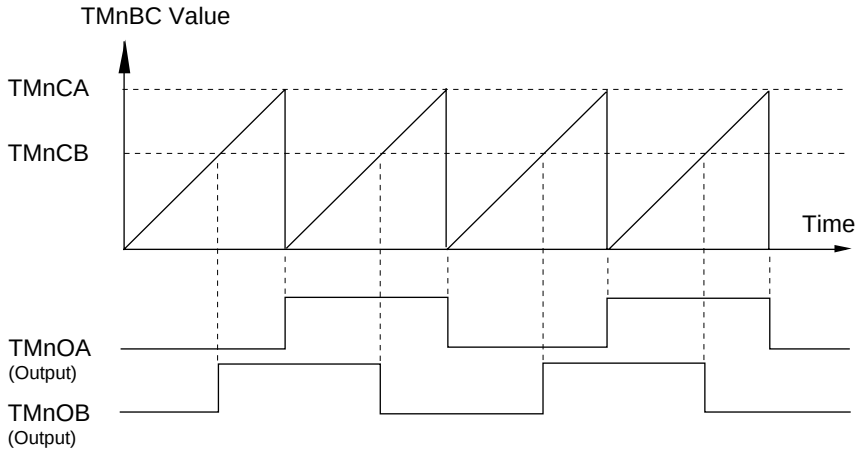


Figure 4-1-5 Two-phase Timer Output Timing (Timer 6 and Timer 7)

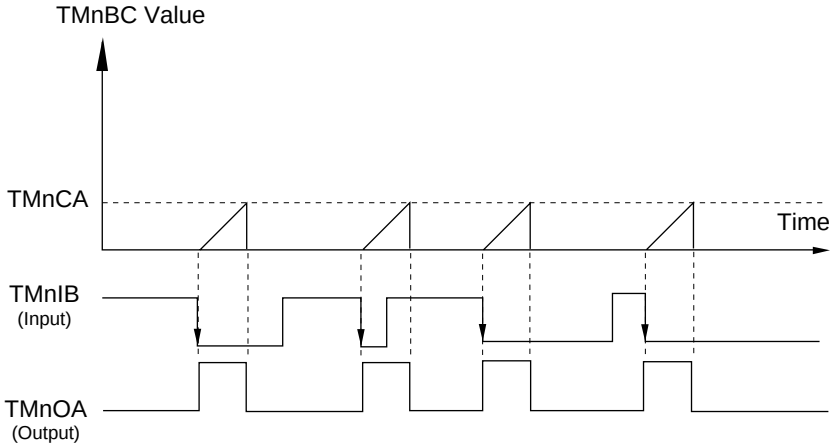


Figure 4-1-6 One-shot Pulse Output Timing (Timer6 and Timer 7)

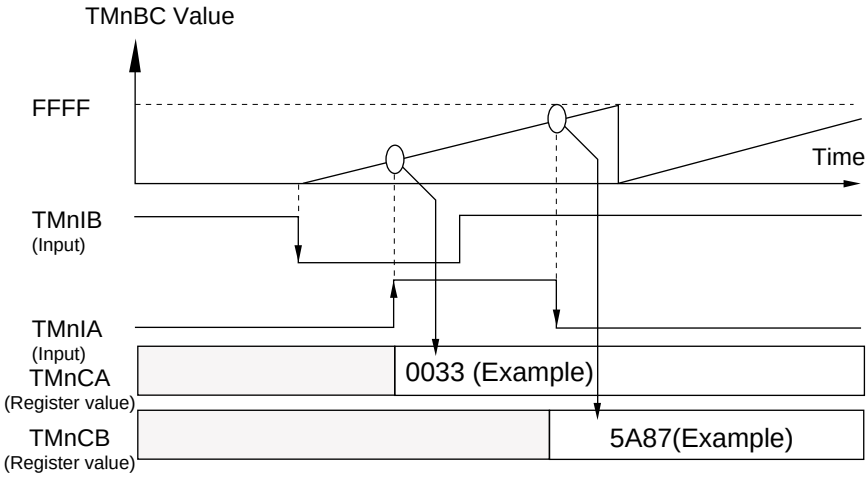


Figure 4-1-7 One-phase Capture Input Timing (Timer6 and Timer 7)

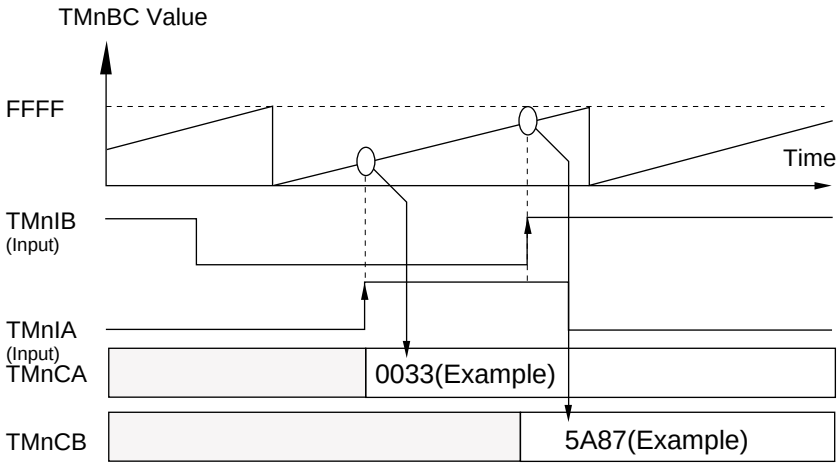


Figure 4-1-8 Two-phase Capture Input Timing (Timer 6 and Timer 7)

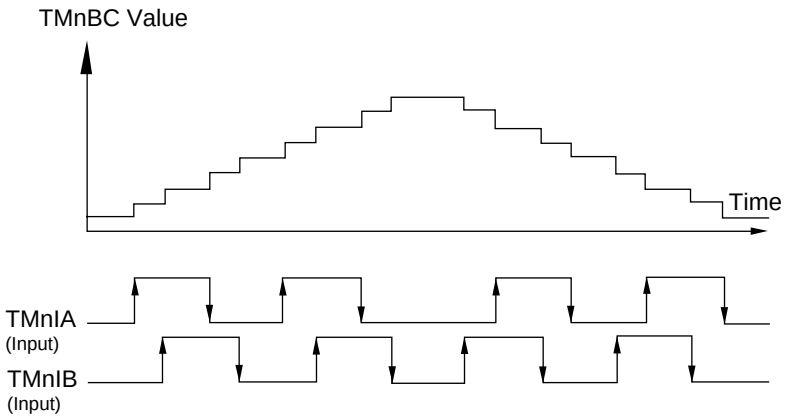


Figure 4-1-9 Two-phase Encoder (4x) Timing

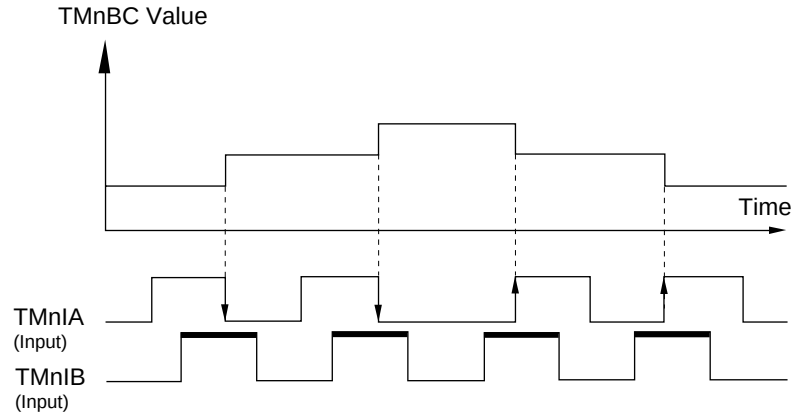


Figure 4-1-10 Two-phase Encoder (1x) Timing (Timer 6 and Timer 7)

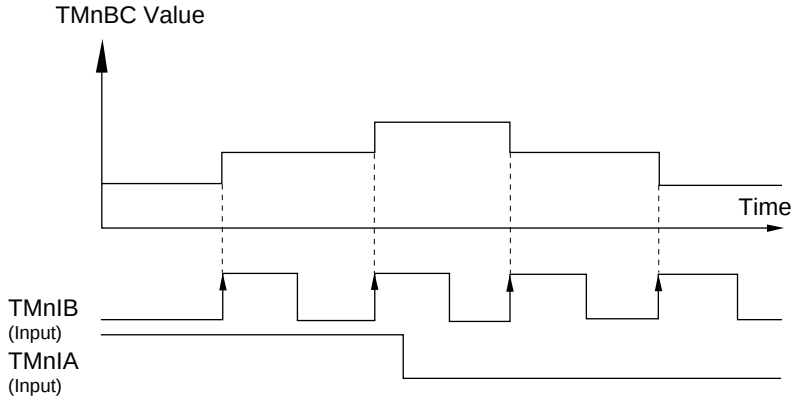


Figure 4-1-11 External Count Direction Control Timing (Timer 6 and Timer 7)

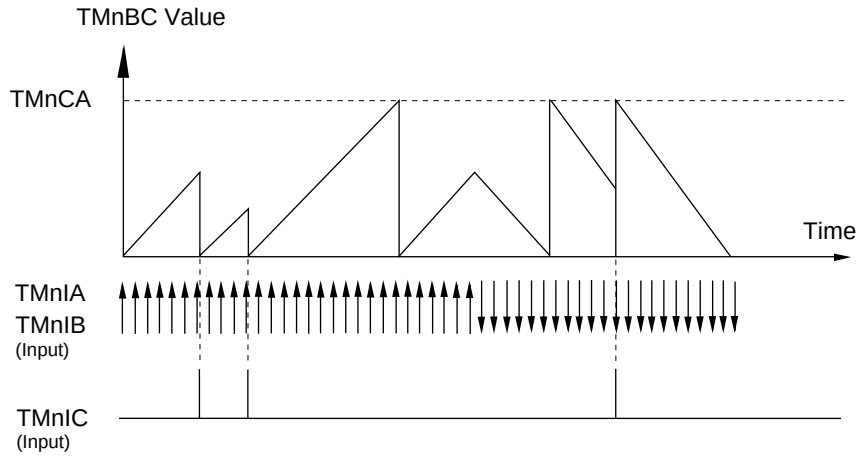


Figure 4-1-12 External Count Reset Control (Two-phase Encoder) Timing (Timer 6 and Timer 7)

Timer 1 to timer 5 can cascade. For example, cascading timer 1 and timer 2 can form as a 16-bit timer. cascading timer 3, timer 4 and timer 5 can form as a 24-bit timer. Cascading these timers can form a 40-bit timer at most.

■ Timer 0 to Timer 5

Timer 0 to Timer 5 are 8-bit timers. They are down counting and are divided by the 8-bit value set in the base register (TMnBR) plus one. (Do not set 0 to TMnBR). An interrupt occurs when each timer underflows (the binary counter changes from xÕ00Õ to the 8-bit value). They can function as interval timers, event counters, clock output, base clock for serial interface and A/D conversion start timing.

■ Timer 6 and Timer 7

Timer 6 and Timer 7 are 16-bit timers. They are up/down counting. Each timer has two compare/capture registers (TMnCA and TMnCB). These registers capture and compare the up/down counter value, generate PWM and interrupts. The PWM contains the double buffer mode that changes the cycle and transition from the next cycle. This prevents the PWM waveform losses and distorts during timing changes. These timers can function as interval timers, event counters (at clock oscillation), one-phase PWM, two-phase PWM, two capture input, dual two-phase encoders, one-shot pulse generators and external count direction controllers.

An underflow interrupt occurs only when these timers are down counting.

Figure 4-1-13 shows the timer configuration. Combining timers serves as various interval timers.

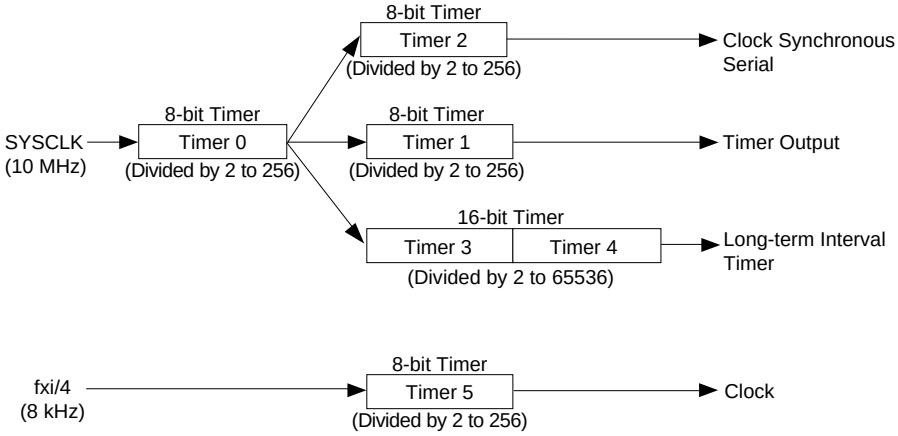


Figure 4-1-13 Timer Configuration

Each timer n (n=2 to 5) cascade inputs cascade output of timer n-1. Therefore, timer does not function as a 8-bit counter but it functions as a 16-bit counter. SYSCLK is a signal of dividing the clock from OSCI pin by 2 (10 MHz with a 20-MHz oscillator) during normal mode or HALT0 mode. SYSCLK becomes a signal of dividing the clock from XI pin by 2 (16 kHz with a 32 kHz oscillator) during SLOW mode or HALT1 mode. SYSCLK stops during STOP0 mode or STOP1 mode. SYSCLK outputs to the external SYSCLK pin. The fxi/4 means a signal of dividing the clock from XI pin by 4 (18 kHz with a 32 kHz oscillator) during modes except STOP0 and STOP1 modes. The fxi/4 stops during STOP0 or STOP1 mode.

4-1-2 Control Registers

The following table shows timer control registers.

Table 4-1-2 List of Timer Control Registers

Register		Address	R/W	Function
Timer 0	TM0MD	x'00FE20'	R/W	Timer 0 Mode Register
	TM0BC	x'00FE00'	R	Timer 0 Binary Counter
	TM0BR	x'00FE10'	R/W	Timer 0 Base Register
Timer 1	TM1MD	x'00FE21'	R/W	Timer 1 Mode Register
	TM1BC	x'00FE01'	R	Timer 1 Binary Counter
	TM1BR	x'00FE11'	R/W	Timer 1 Base Register
Timer 2	TM2MD	x'00FE22'	R/W	Timer 2 Mode Register
	TM2BC	x'00FE02'	R	Timer 2 Binary Counter
	TM2BR	x'00FE12'	R/W	Timer 2 Base Register
Timer 3	TM3MD	x'00FE23'	R/W	Timer 3 Mode Register
	TM3BC	x'00FE03'	R	Timer 3 Binary Counter
	TM3BR	x'00FE13'	R/W	Timer 3 Base Register
Timer 4	TM4MD	x'00FE24'	R/W	Timer 4 Mode Register
	TM4BC	x'00FE04'	R	Timer 4 Binary Counter
	TM4BR	x'00FE14'	R/W	Timer 4 Base Register
Timer 5	TM5MD	x'00FE25'	R/W	Timer 5 Mode Register
	TM5BC	x'00FE05'	R	Timer 5 Binary Counter
	TM5BR	x'00FE15'	R/W	Timer 5 Base Register
Timer 6	TM6MD	x'00FE30'	R/W	Timer 6 Mode Register
	TM6BC	x'00FE32'	R	Timer 6 Binary Counter
	TM6CA	x'00FE34'	R/W	Timer 6 Compare/Capture Register A
	TM6CAX	x'00FE36'	-	Timer 6 Compare/Capture Register Set A
	TM6CB	x'00FE38'	R/W	Timer 6 Compare/Capture Register B
	TM6CBX	x'00FE3A'	-	Timer 6 Compare/Capture Register Set B
Timer 7	TM7MD	x'00FE40'	R/W	Timer 7 Mode Register
	TM7BC	x'00FE42'	R	Timer 7 Binary Counter
	TM7CA	x'00FE44'	R/W	Timer 7 Compare/Capture Register A
	TM7CAX	x'00FE46'	-	Timer 7 Compare/Capture Register Set A
	TM7CB	x'00FE48'	R/W	Timer 7 Compare/Capture Register B
	TM7CBX	x'00FE4A'	-	Timer 7 Compare/Capture Register Set B

The TM6CAX register, the TM6CBX register, the TM7CAX register and the TM7CBX register are dummy registers to specify the double buffer mode when the PWM is output.

4-1-3 Timer Block Diagram

This section describes block diagrams of timer 0 to timer 7.

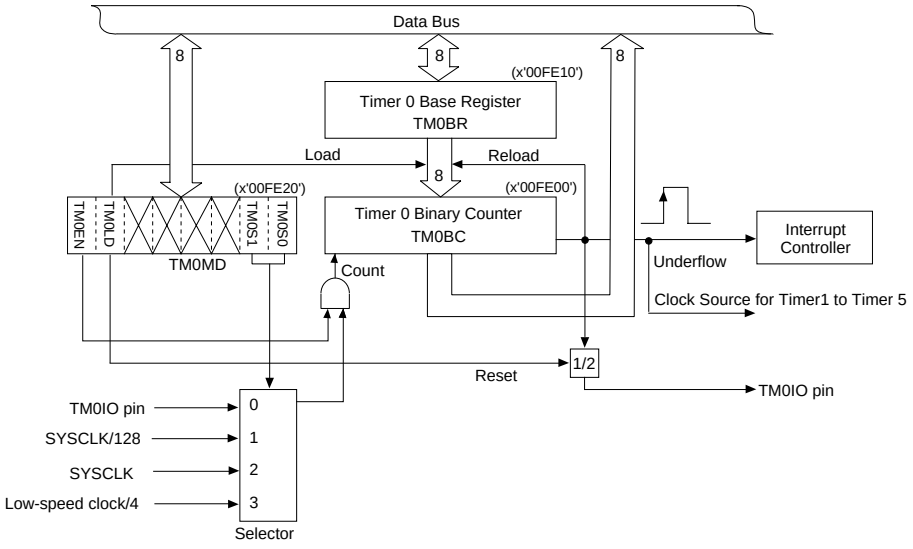


Figure 4-1-14 Timer 0 Block Diagram

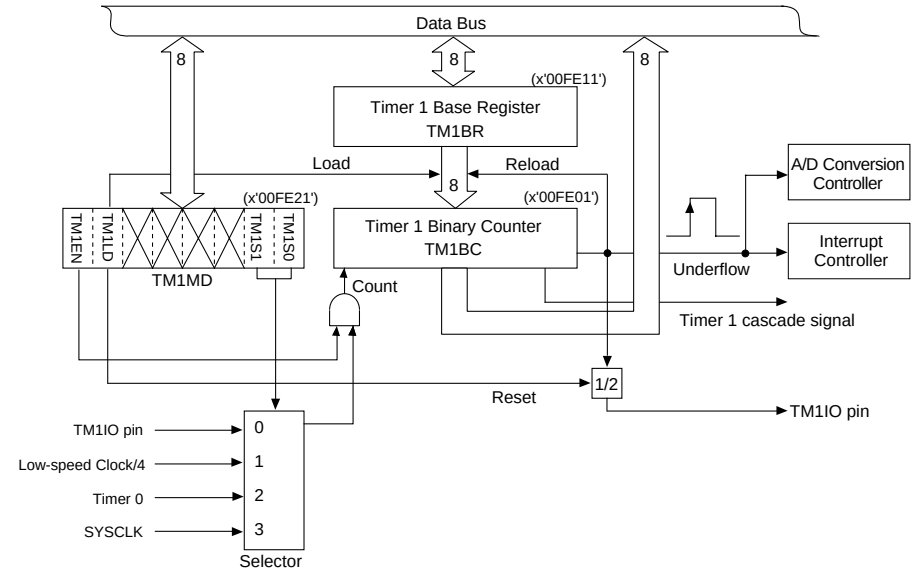


Figure 4-1-15 Timer 1 Block Diagram

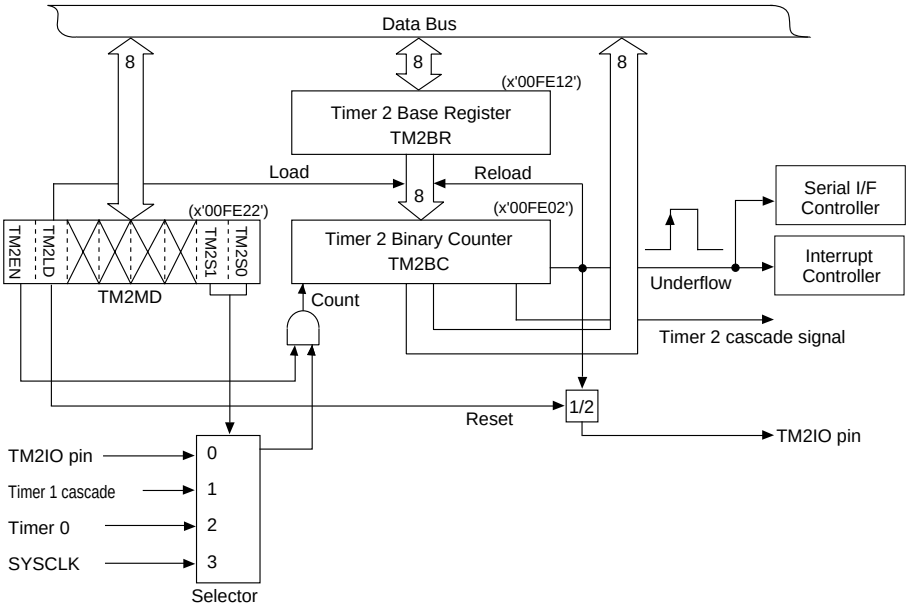


Figure 4-1-16 Timer 2 Block Diagram

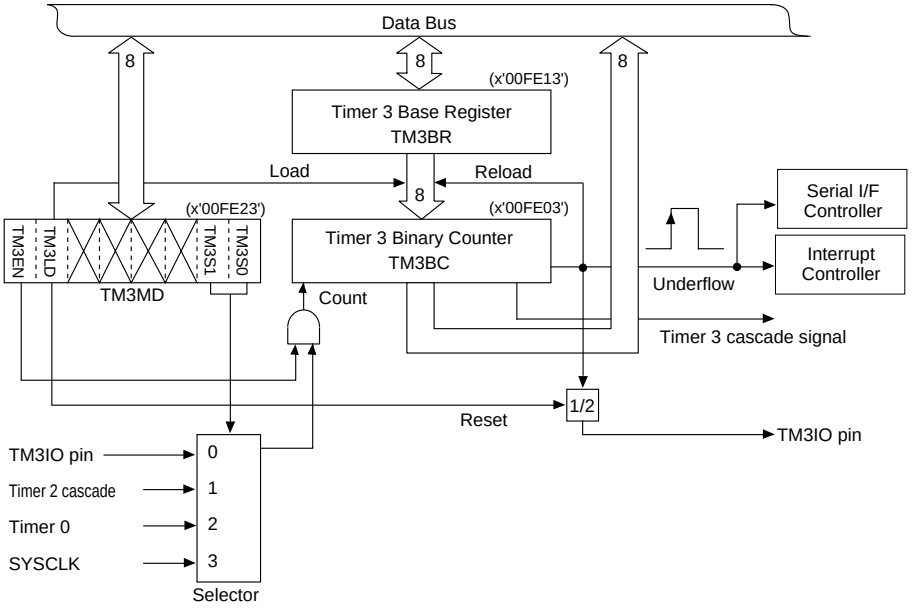


Figure 4-1-17 Timer 3 Block Diagram

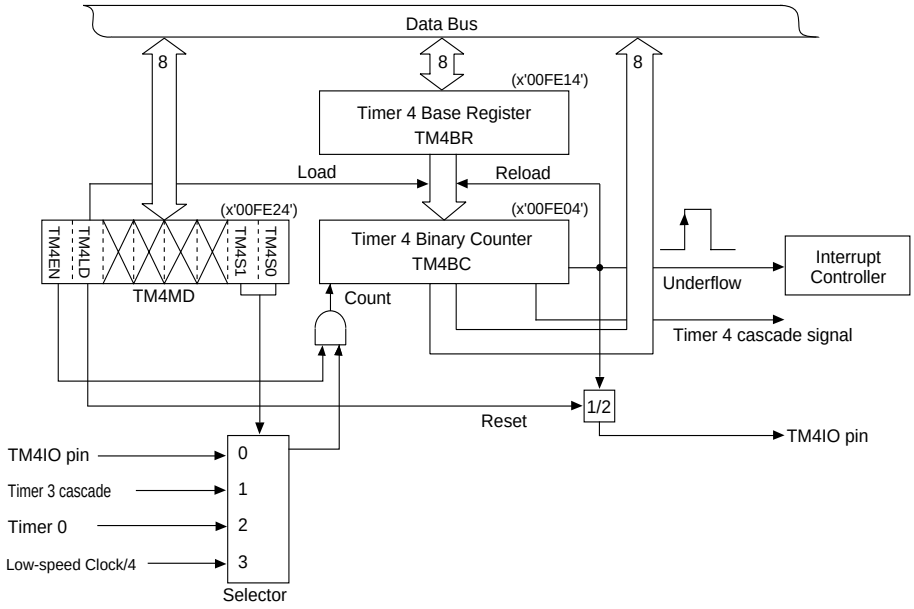


Figure 4-1-18 Timer 4 Block Diagram

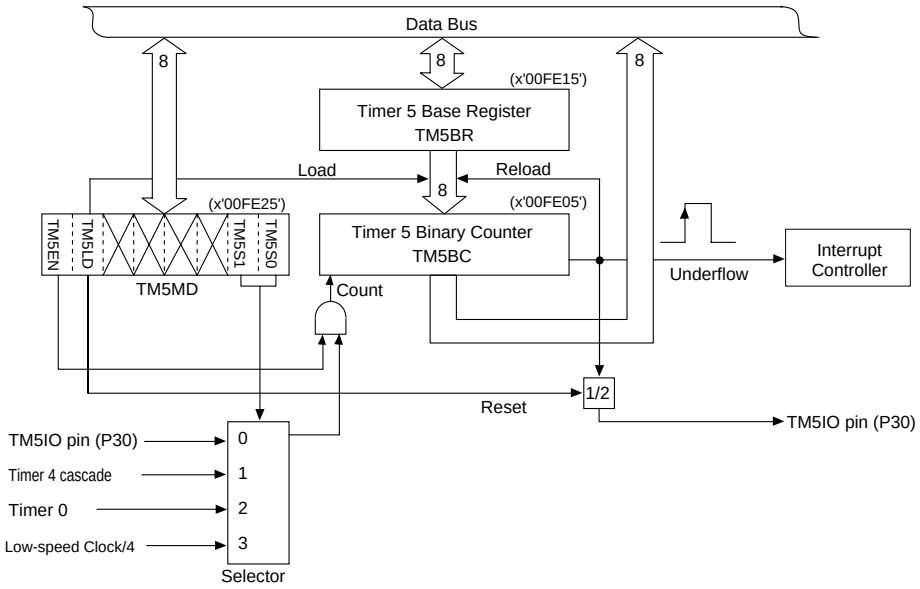


Figure 4-1-19 Timer 5 Block Diagram

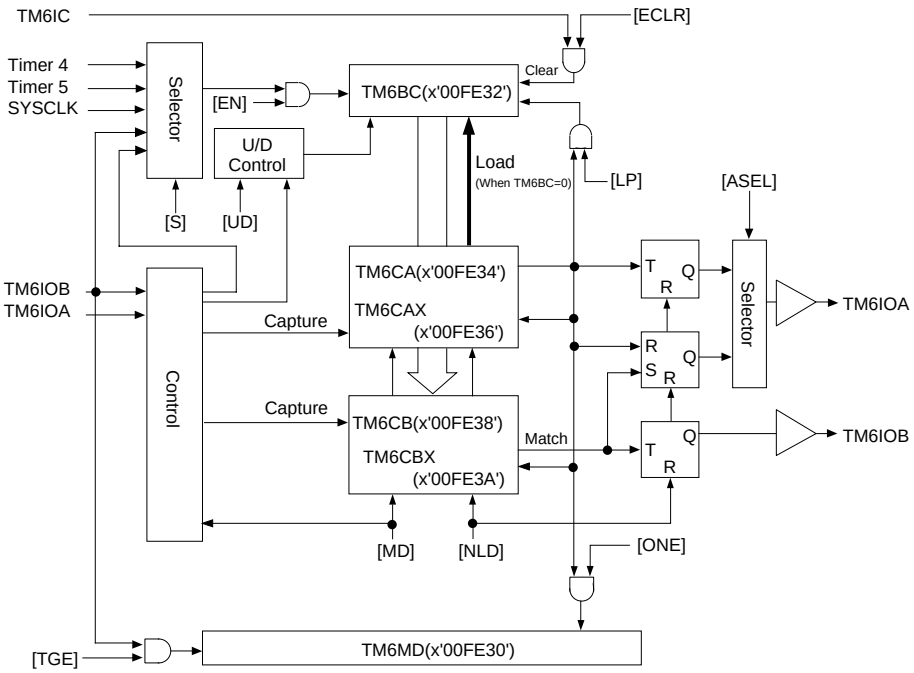


Figure 4-1-20 Timer 6 Block Diagram

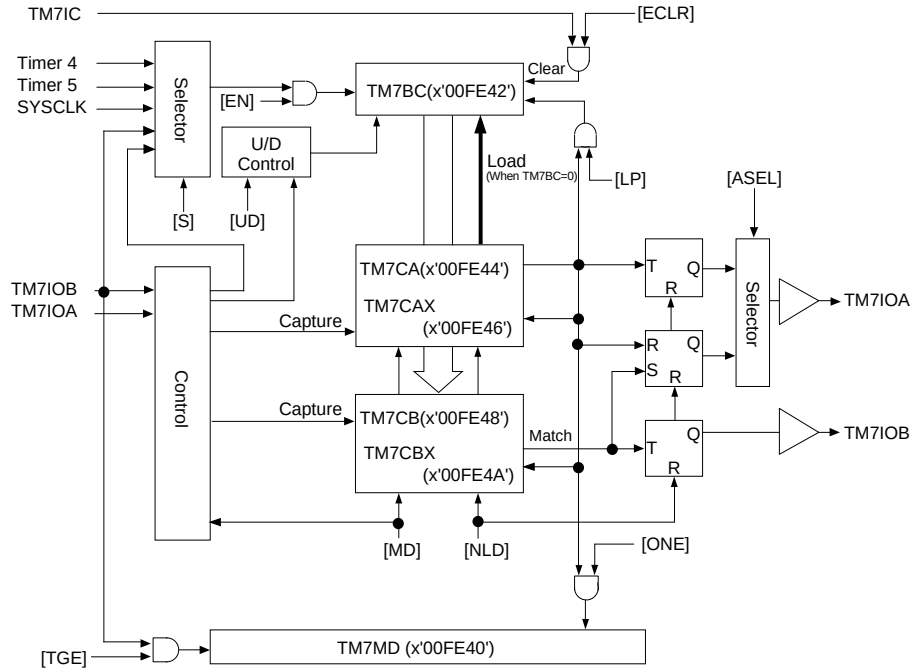


Figure 4-1-21 Timer 7 Block Diagram

4-2 8-bit Timer Setup Examples

4-2-1 Event Counter Using 8-bit Timer

The event counter setup procedures for Timer 0 to Timer 5 are the same. In this example, timer 2 counts the rising edge of the TM2IO pin input four times and generates an interrupt at underflow.

(1) Set the interrupt enable flag (IE) of the processor status word (PSW) to 1.

This verification is unnecessary immediately after a reset.

(2) Verify that counting is stopped using the timer 2 mode register (TM2MD).

TM2MD: x'00FE22'

7	6	5	4	3	2	1	0
TM2 EN	TM2 LD	-	-	-	-	TM2 S1	TM2 S0
0	0	-	-	-	-	0	0

(3) Enable interrupts. At the same time, clear all prior interrupt requests. Set G3LV[2:0] bits of the maskable interrupt control register 3 (G3ICR) to the interrupt level of 6 to 0, TM2IR and TM2IE to 0 and 1, respectively. For example, write x'4200' to the G3ICR register. Thereafter, an interrupt occurs when timer 2 underflows.

G3ICR: x'00FC46'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G3 LV2	G3 LV1	G3 LV0	SC0R IE	SC0T IE	TM2 IE	IRQ2 IE	SC0R IR	SC0T IR	TM2 IR	IRQ2 IR	SC0R ID	SC0T ID	TM2 ID	IRQ2 ID
-	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

(4) Set the timer divisor. Since timer 2 divides the TM2IO pin by 4, set the timer 2 base register (TM2BR) to 3. (The valid range for TM2BR is 1 to 255.)

TM2BR: x'00FE12'

7	6	5	4	3	2	1	0
TM2 BR7	TM2 BR6	TM2 BR5	TM2 BR4	TM2 BR3	TM2 BR2	TM2 BR1	TM2 BR0
0	0	0	0	0	0	1	1

(5) Load the TM2BR value to the TM2BC register. To do this, set TM2LD and TM2EN of the TM2MD register to 1 and 0 respectively. At the same time, select the clock source. Set TM2S[1:0] to 00.

(6) Set both TM2LD and TM2EN of the TM2MD register to 0. If this setting is omitted, the timer 2 binary counter may not start at the first cycle.

(7) Set both TM2LD and TM2EN to 0. This starts timer 2. Counting starts at the beginning of the next cycle.

Changing the clock source while controlling count operation will corrupt the binary counter value.

When the timer 2 binary counter value reaches 0 and loads the value of 3 from the timer 2 base register (TM2BR), a timer 2 underflow interrupt request occurs.

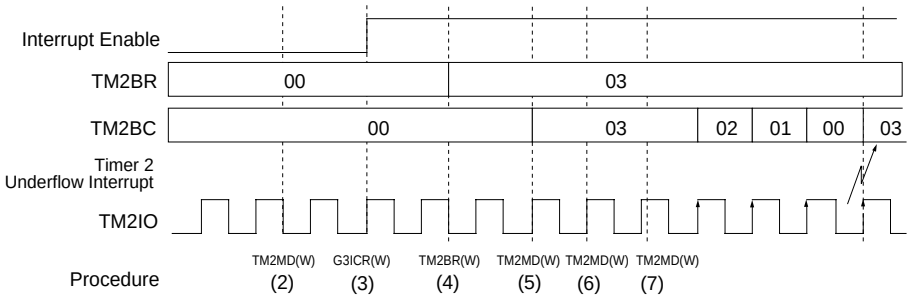


Figure 4-2-1 Event Counter Timing

4-2-2 Clock Output Using 8-bit Timer

Timer 0 to timer 5 contain clock output functions. The setup procedures for timer 0 to timer 5 are same. In this example, timer 0 and timer 1 output 12 clock cycles (SYSCLK/6).

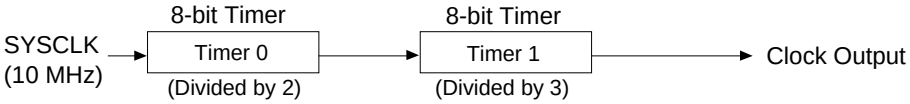


Figure 4-2-2 Clock Output Configuration (1)

■ Timer 0 Setup

(1) Verify that timer 0 counting is stopped using the timer 0 mode register (TM0MD).

This verification is unnecessary immediately after a reset.

TM0MD: x'00FE20'

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	-	-	-	-	TM0 S1	TM0 S0
0	1					1	0

(2) Set the timer 0 divisor. Since timer 0 divides SYSCLK by 2, set the timer 0 base register (TM0BR) to 1. (The valid range for TM0BR is 1 to 255.)

If setting 1 of divisor, write the dummy value (for example, x'0F') once.

TM0BR: x'00FE10'

7	6	5	4	3	2	1	0
TM0 BR7	TM0 BR6	TM0 BR5	TM0 BR4	TM0 BR3	TM0 BR2	TM0 BR1	TM0 BR0
0	0	0	0	0	0	0	1

(3) Load the TM0BR value to TM0BC. To do this, set TM0LD and TM0EN to 1 and 0 resepctively.

TM0MD: x'00FE20'

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	-	-	-	-	TM0 S1	TM0 S0
0	1					1	0

(4) Set both TM0LD and TM0EN of the TM0MD register to 0. If this setting is omitted, the timer 0 binary counter may not start at the first cycle.

(5) Set TM0LD and TM0EN to 0 and 1 respectively. This starts timer 0. Counting starts at the beginning of the next cycle. When the timer 0 binary counter value reaches 0 and loads the value of 1 from the timer 0 base register (TM0BR), a timer 0 underflow interrupt request occurs.

If selecting 1 of divisor, set 0 to the timer 0 base register (TM0BR) once again after step (5). The first count is the value set in step (2), but the second count becomes 1. For example, if 0 is set to TM0BR in step (2), the first count is 257 and the second count becomes 1.

■ Pin Setup

(6) Select the TM1IO pin to output using the port 8 I/O control register (P8DIR) and the port 8 output mode register (P8MD). (The set value is 2.)

P8DIR: x'00FFE8'

7	6	5	4	3	2	1	0
P8 DIR7	P8 DIR6	P8 DIR5	P8 DIR4	P8 DIR3	P8 DIR2	P8 DIR1	P8 DIR0
0	0	0	0	0	0	1	0

P8MD: x'00FFF8'

7	6	5	4	3	2	1	0
P8 MD7	P8 MD6	P8 MD5	P8 MD4	P8 MD3	P8 MD2	P8 MD1	P8 MD0
0	0	0	0	0	0	1	0

■ Timer 1 Setup

(7) Verify that timer 1 counting is stopped using the timer 1 mode register (TM1MD).

This verification is unnecessary immediately after a reset.

TM1MD: x'00FE21'

7	6	5	4	3	2	1	0
TM1 EN	TM1 LD	-	-	-	-	TM1 S1	TM1 S0
0	0					1	0

(8) Set the timer 1 divisor. Since timer 1 divides timer 0 output by 3, set the timer 1 base register (TM1BR) to 2. (The valid range for TM0BR is 1 to 255.)

TM1BR: x'00FE11'

7	6	5	4	3	2	1	0
TM1 BR7	TM1 BR6	TM1 BR5	TM1 BR4	TM1 BR3	TM1 BR2	TM1 BR1	TM1 BR0
0	0	0	0	0	0	1	0

(9) Load the TM1BR value to TM1BC. To do this, set TM1LD and TM1EN to 1 and 0 resepctively. At the same time, select the clock source.

Changing the clock source while controlling count operation will corrupt the binary counter value.

(10) Set both TM1LD and TM1EN of the TM1MD register to 0. If this setting is omitted, the timer 0 binary counter may not start at the first cycle.

(11) Set TM1LD and TM1EN to 0 and 1 respectively. This starts timer 1. Counting starts at the beginning of the next cycle.

When the TM1BC value reaches 0, TM1IO output is inverted as soon as the value of 2 from the timer 1 base register (TM1BR) is loaded. Immediately after TM1BC starts counting, the TM1IO output pin outputs 0. The TM1IO output pin outputs 1 at the beginning of the next cycle when TM1BC becomes 0. Then the TM1IO output pin outputs 0 again at the beginning of the next cycle. This repeated operation results in 12 clock cycles.

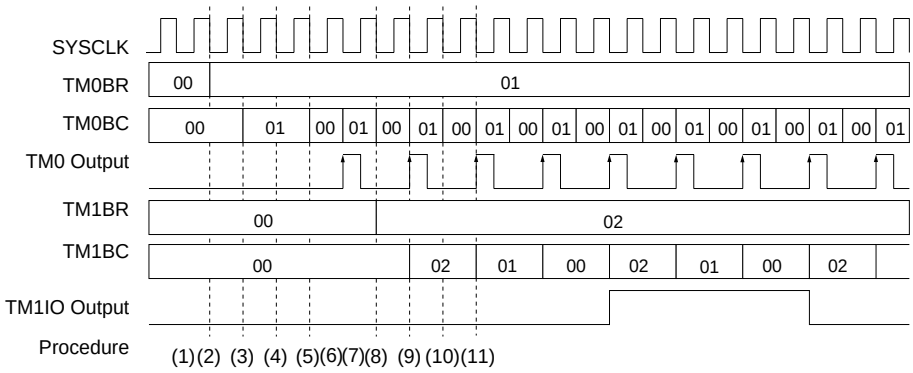


Figure 4-2-3 Clock Output Timing

4-2-3 Interval Timer Using 8-bit Timer

The interval timer setup procedures for timer 0 to timer 5 are same. In this example, timer 0, timer 2 and timer 3 generate an interrupt at regular intervals (1 second). (To divide SYSCLK by 10,000,000, timer 0 divides SYSCLK by 250 and timer 2 and timer 3 divide SYSCLK by 40,000.)

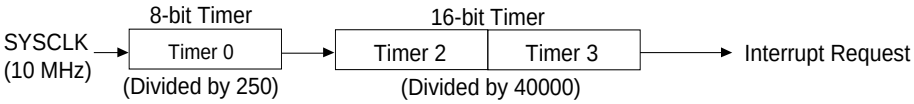


Figure 4-2-4 Clock Output Configuration (2)

(1) Set the interrupt enable flag (IE) of the processor status word (PSW) to 1.

(2) Enable interrupts. At the same time, clear all prior interrupt requests. Set G4LV[2:0] bits of the maskable interrupt control register 4 (G4ICR) to the interrupt level of 6 to 0, TM3IR and TM3IE to 0 and 1, respectively. For example, write x'4200' to the G4ICR register. Thereafter, an interrupt occurs when timer 3 underflows.

G4ICR: x'00FC48'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G4 LV2	G4 LV1	G4 LV0	SC1R IE	SC1T IE	TM3 IE	IRQ3 IE	SC1R IR	SC1T IR	TM3 IR	IRQ3 IR	SC1R ID	SC1T ID	TM3 ID	IRQ3 ID
-	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

■ Timer 0 Setup

(3) Verify that timer 0 counting is stopped using the timer 0 mode register (TM0MD).

This verification is unnecessary immediately after a reset.

TM0MD: x'00FE20'

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	-	-	-	-	TM0 S1	TM0 S0
0	0					1	0

(2) Set the timer 0 divisor. Since timer 0 divides SYSCLK by 250, set the timer 0 base register (TM0BR) to 249. (The valid range for TM0BR is 1 to 255.)

If setting 1 of divisor, write the dummy value (for example, x'0F') once.

TM0BR: x'00FE10'

7	6	5	4	3	2	1	0
TM0 BR7	TM0 BR6	TM0 BR5	TM0 BR4	TM0 BR3	TM0 BR2	TM0 BR1	TM0 BR0
1	1	1	1	1	0	0	1

(5) Load the TM0BR value to TM0BC. To do this, set TM0LD and TM0EN to 1 and 0 resepctively.

TM0MD: x'00FE20'

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	-	-	-	-	TM0 S1	TM0 S0
0	0					1	0

(6) Set both TM0LD and TM0EN of the TM0MD register to 0. If this setting is omitted, the timer 0 binary counter may not start at the first cycle.

If selecting 1 of divisor, set 0 to the timer 0 base register (TM0BR) once again after step (7). The first count is the value set in step (4), but the second count becomes 1. For example, if 0 is set to TM0BR in step (4), the first count is 257 and the second count becomes 1.

(7) Set TM0LD and TM0EN to 0 and 1 respectively. This starts timer 0. Counting starts at the beginning of the next cycle. When the timer 0 binary counter (TM0BC) reaches 0 and loads the value of 1 from the timer 0 base register (TM0BR), a timer 0 underflow interrupt request occurs.

■ Timer 2 and Timer 3 Setup

(8) Verify that counting is stopped using the timer 2 mode register (TM2MD) and the timer 3 mode register (TM3MD).

This verification is unnecessary immediately after a reset.

TM2MD: x'00FE22'

7	6	5	4	3	2	1	0
TM2 EN	TM2 LD	-	-	-	-	TM2 S1	TM2 S0
0	0	-	-	-	-	0	0

TM3MD: x'00FE23'

7	6	5	4	3	2	1	0
TM3 EN	TM3 LD	-	-	-	-	TM3 S1	TM3 S0
0	0					0	1

(9) Set the timer divisor. Since the divisor is 40000 (x'9C40'), set the timer 2 base register (TM2BR) and the timer 3 base register (TM3BR) to x'3F' and x'9C'. (The valid range is 1 to 255.)

TM2BR: x'00FE12'

7	6	5	4	3	2	1	0
TM2 BR7	TM2 BR6	TM2 BR5	TM2 BR4	TM2 BR3	TM2 BR2	TM2 BR1	TM2 BR0
0	0	1	1	1	1	1	1

TM3BR: x'00FE13'

7	6	5	4	3	2	1	0
TM3 BR7	TM3 BR6	TM3 BR5	TM3 BR4	TM3 BR3	TM3 BR2	TM3 BR1	TM3 BR0
1	0	0	1	1	1	0	0

(10) Load the TM2BR value to TM2BC and the TM3BR to TM3BC. To do this, set both TM2LD and TM3LD to 1, and both TM2EN and TM3EN to 0. At the same time, select the clock sources. (Select timer 0 for the timer 2 clock source and timer 2 cascade for the timer 3 clock source.)

Changing the clock source while controlling count operation will corrupt the binary counter value.

(11) Set both TM2LD and TM3LD to 0, and both TM2EN and TM3EN to 0. If this setting is omitted, the binary counter may not start at the first cycle.

(12) Set TM2LD and TM3LD to 0, and TM2EN and TM3EN to 1. This starts the timer. Counting starts at the beginning of the next cycle.

When the TM2BC value and the TM3BC value reache 0, a timer 3 underflow interrupt request occurs as soon as the TM2BR value x'3F' and the TM3BR value x'9C' are loaded.

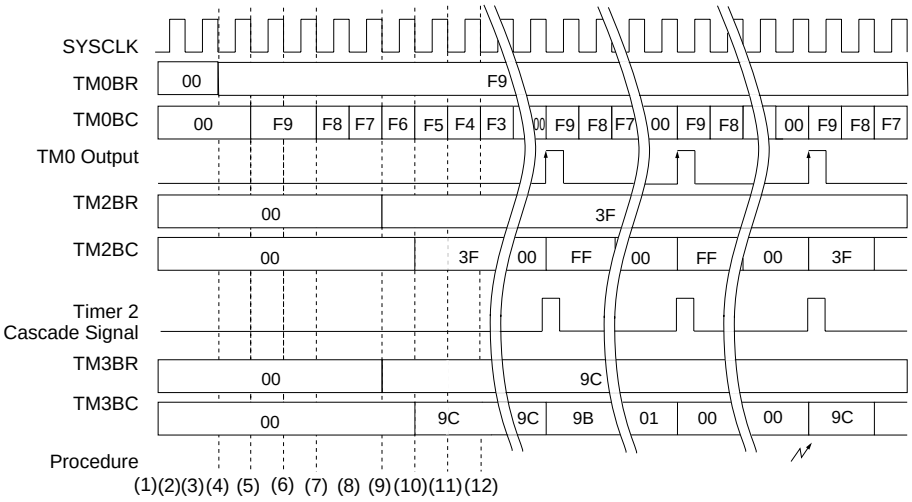


Figure 4-2-5 Interval Timer Timing

4-3 16-bit Timer Setup Examples

4-3-1 Event Counter Using 16-bit Timer

The event counter setup procedures for Timer 6 and Timer 7 are same except the up/down counting selection. In this example, timer 6 counts TM6IOB pin input (SYSCLK/2 or less, 5 MHz or less with a 20-MHz oscillaor) and generates an interrupt on the second cycle and fifth cycle.

Use the MOV instruction to set the data and always use 16-bit write operations.

■ Interrupt Enable Setup

(1) Enable interrupts. At the same time, clear all prior interrupt requests. Set G6LV[2:0] bits of the G6ICR to the interrupt level of 6 to 0, TM6AIR and TM6BIR to 0, and TM6AIE and TM6BIE to 1. For example, write xÕ4600Õ to the G6ICR register. Thereafter, an interrupt occurs when the timer 6 capture A and the timer 6 capture B occur.

■ Timer 6 Setup

Stop TM6BC counting and initialize (clear) TM6BC and RS.F.F.

(2) Set the operating mode to the timer 6 mode register (TM6MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Select TM6IOB as the timer 6 clock source.

TM6MD: x'00FE30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 EN	TM6 NLD	-	-	TM6 UD1	TM6 UD0	TM6 TGE	TM6 ONE	TM6 MD1	TM6 MD0	TM6 ECLR	TM6 LP	TM6 ASEL	TM6 S2	TM6 S1	TM6 S0
0	0	-	-	0	0	0	0	0	0	0	1	0	0	1	0

(3) Set the timer 6 divisor. Since timer 6 divides TM6IOB pin input by 5, set 4 to the timer 6 compare/capture register A (TM6CA). (The valid range for TM6CA is 1 to x'FFFE'.)

TM6CA: x'00FE34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CA15	TM6 CA14	TM6 CA13	TM6 CA12	TM6 CA11	TM6 CA10	TM6 CA9	TM6 CA8	TM6 CA7	TM6 CA6	TM6 CA5	TM6 CA4	TM6 CA3	TM6 CA2	TM6 CA1	TM6 CA0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

In the single buffer mode, both TM6CA and TM6CB are compared to TM6BC.

(4) Set the phase difference for timer 6. Since the phase difference is 2 cycles, set 1 to the timer 6 compare/capture register B (TM6CB). (The valid range for TM6CB is -1 ² TM6CB < TM6CA.)

The TM6CB value is set to '-1' by writing x'FFFF' to TM6CB. When TM6CB is not compared to TM6BC, the TM6CB value is set to '-1'.

TM6CB: x'00FE38'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CB15	TM6 CB14	TM6 CB13	TM6 CB12	TM6 CB11	TM6 CB10	TM6 CB9	TM6 CB8	TM6 CB7	TM6 CB6	TM6 CB5	TM6 CB4	TM6 CB3	TM6 CB2	TM6 CB1	TM6 CB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(5) Set TM6NLD and TM6EN of the timer 6 mode register (TM6MD) to 1 and 0 respectively. This enables TM6BC, T.F.F and RS.F.F.

TM6MD: x'00FE30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 EN	TM6 NLD	-	-	TM6 UD1	TM6 UD0	TM6 TGE	TM6 ONE	TM6 MD1	TM6 MD0	TM6 ECLR	TM6 LP	TM6 ASEL	TM6 S2	TM6 S1	TM6 S0
0	1	-	-	0	0	0	0	0	0	0	1	0	0	1	0

(6) Set both TM6NLD and TM6EN to 1. This starts the timer 6. Counting starts at the beginning of the next cycle.

If this step is omitted, TM6BC may not count during the first cycle. Do not change other bits in the TM6MD register at the same time.

When SYSCLK operates (in normal and halt modes), the external TM6IOB input is sampled on SYSCLK. When SYSCLK stops (in STOP mode), TM6BC counts on the TM6IOB input. Select the oscillation clock/4 (5 MHz with a 20-MHz oscillator) or less as the event counter clock. Figure 4-3-1 shows the example of generating an interrupt during up counting.

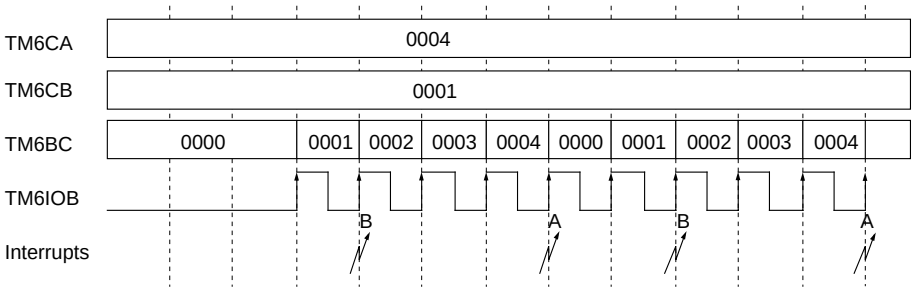


Figure 4-3-1 Event Counter Timing

4-3-2 PWM Output Using 16-bit Timer

The PWM output setup procedures for Timer 6 and Timer 7 are same except the up/down counting selection. In this example, timer 6 divides SYSCLK by 5 and outputs PWM signal on the fifth cycle. The duty is 2:3. Therefore, set the divisor of 5 (the set value is '4') to the timer 6 compare/capture register A and the cycle of 2 (the set value is '1') to the timer 6 compare/capture B.

■ Pin Setup

(1) Set the TM6IOA pin to output using the port 8 I/O control register (P8DIR) and the port 8 output mode register (P8MD).

P8DIR: x'00FFE8'

7	6	5	4	3	2	1	0
P8 DIR7	P8 DIR6	P8 DIR5	P8 DIR4	P8 DIR3	P8 DIR2	P8 DIR1	P8 DIR0
0	1	0	0	0	0	0	0

P8MD: x'00FFF8'

7	6	5	4	3	2	1	0
P8 MD7	P8 MD6	P8 MD5	P8 MD4	P8 MD3	P8 MD2	P8 MD1	P8 MD0
0	1	0	0	0	0	0	0

■ Timer 6 Setup

(2) Set the operating mode to the timer 6 mode register (TM6MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Select SYSCLK as the timer 6 clock source. Select the double buffer operating mode.

Use the MOV instruction to set the data and always use 16-bit write operations.

Stop TM6BC counting and initialize (clear) TM6BC and RS.F.F.

TM6MD: x'00FE30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 EN	TM6 NLD	-	-	TM6 UD1	TM6 UD0	TM6 TGE	TM6 ONE	TM6 MD1	TM6 MD0	TM6 ECLR	TM6 LP	TM6 ASEL	TM6 S2	TM6 S1	TM6 S0
0	0	-	-	0	0	0	0	0	1	0	1	0	0	1	1

(3) Set the timer 6 divisor. Since timer 6 divides SYSCLK by 5, set 4 to the timer 6 compare/capture register A (TM6CA). (The valid range for TM6CA is 1 to x'FFFE'.)

TM6CA: x'00FE34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CA15	TM6 CA14	TM6 CA13	TM6 CA12	TM6 CA11	TM6 CA10	TM6 CA9	TM6 CA8	TM6 CA7	TM6 CA6	TM6 CA5	TM6 CA4	TM6 CA3	TM6 CA2	TM6 CA1	TM6 CA0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

(4) Set the timer 6 duty. Since the duty is 2/5 of SYSCLK, set 1 to the timer 6 compare/capture register B (TM6CB). (The valid range for TM6CB is -1 ² TM6CB < TM6CA.)

The TM6CB value is set to '-1' by writing x'FFFF' to TM6CB. When TM6CB is not compared to TM6BC, the TM6CB value is set to '-1'.

TM6CB: x'00FE38'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CB15	TM6 CB14	TM6 CB13	TM6 CB12	TM6 CB11	TM6 CB10	TM6 CB9	TM6 CB8	TM6 CB7	TM6 CB6	TM6 CB5	TM6 CB4	TM6 CB3	TM6 CB2	TM6 CB1	TM6 CB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(5) In the double buffer mode, compare TM6BC to TM6CAX. The TM6CAX is updated when TM6CAX = TM6BC, so that TM6CAX remains x'0000' before TM6BC starts counting. Therefore, to load the TM6CA value to TM6CAX, write the dummy data to TM6CAX. (The dummy data can be any values.)

TM6CAX and TM6CBX are valid only when the timer 6 compare/capture register is set to double buffer mode.

TM6CAX: x'00FE36'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CAX15	TM6 CAX14	TM6 CAX13	TM6 CAX12	TM6 CAX11	TM6 CAX10	TM6 CAX9	TM6 CAX8	TM6 CAX7	TM6 CAX6	TM6 CAX5	TM6 CAX4	TM6 CAX3	TM6 CAX2	TM6 CAX1	TM6 CAX0

(6) In the double buffer mode, compare TM6BC to TM6CBX. The TM6CBX is updated when TM6CBX = TM6BC, so that TM6CBX remains x'0000' before TM6BC starts counting. Therefore, to load the TM6CA value to TM6CBX, write the dummy data to TM6CBX. (The dummy data can be any values.)

TM6CBX: x'00FE3A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CBX15	TM6 CBX14	TM6 CBX13	TM6 CBX12	TM6 CBX11	TM6 CBX10	TM6 CBX9	TM6 CBX8	TM6 CBX7	TM6 CBX6	TM6 CBX5	TM6 CBX4	TM6 CBX3	TM6 CBX2	TM6 CBX1	TM6 CBX0

The setup steps after step (6) are the same as steps (5) and (6) in '4-3-1 Event Counter Using 16-bit Timer'.

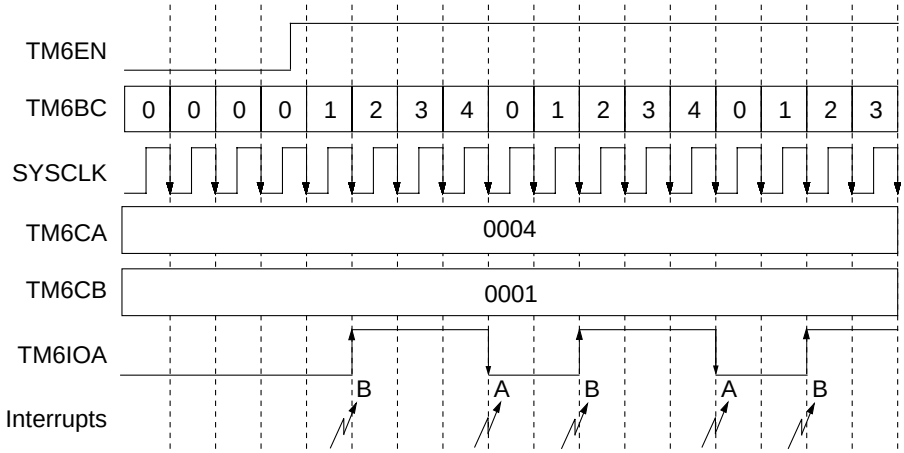


Figure 4-3-2 PWM Timing

When timer n changes the duty of PWM output waveforms dynamically, the PWM output waveforms and interrupts may corrupt at the timing of changing the TMnCB value in the single buffer mode. In the double buffer mode, the corrupt of PWM output waveforms and interrupts does not occur at any timing of changing the TMnCB value. This corrupt does not occur even when the output waveforms consist of 1s and 0s.

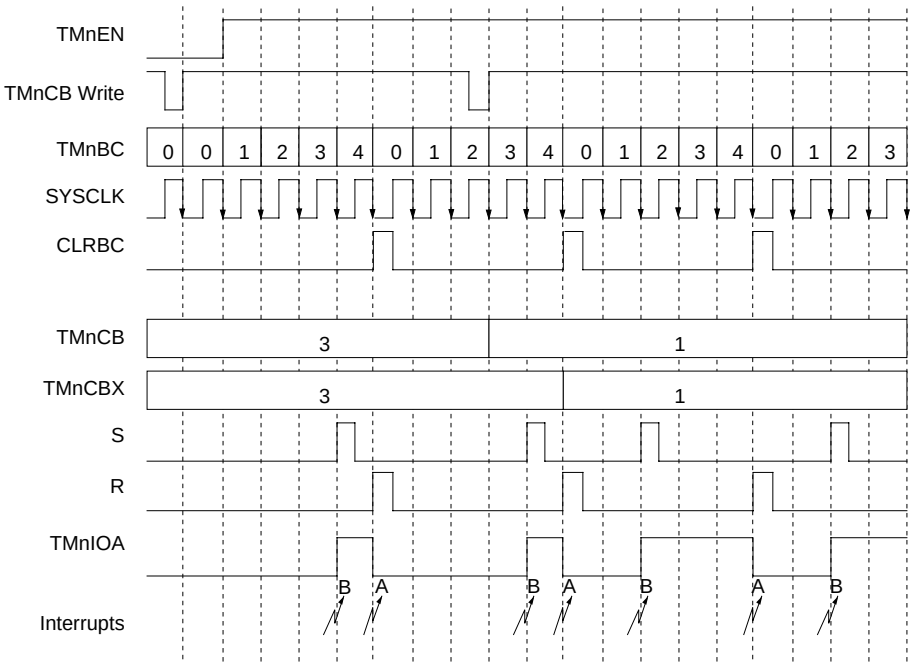


Figure 4-3-3 PWM Timing in Double Buffer Mode

4-3-3 Two-phase PWM Output Using 16-bit Timer

The two-phase PWM output setup procedures for Timer 6 and Timer 7 are same except the up/down counting selection. In this example, timer 6 divides SYSCLK by 5 and outputs two-phase PWM signal on the fifth cycle. The phase difference is 2 cycles. Therefore, set the divisor of 5 (the set value is '4') to the timer 6 compare/capture register A and the cycle of 2 (the set value is '1') to the timer 6 compare/capture B.

■ Pin Setup

(1) Set the TM6IOA pin to output using the port 8 I/O control register (P8DIR) and the port 8 output mode register (P8MD).

This verification is unnecessary immediately after a reset.

P8DIR: x'00FFE8'

7	6	5	4	3	2	1	0
P8 DIR7	P8 DIR6	P8 DIR5	P8 DIR4	P8 DIR3	P8 DIR2	P8 DIR1	P8 DIR0
0	1	0	0	0	0	0	0

P8MD: x'00FFF8'

7	6	5	4	3	2	1	0
P8 MD7	P8 MD6	P8 MD5	P8 MD4	P8 MD3	P8 MD2	P8 MD1	P8 MD0
0	1	0	0	0	0	0	0

■ Timer 6 Setup

(2) Set the operating mode to the timer 6 mode register (TM6MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Select TM6IOB as the timer 6 clock source.

Use the MOV instruction to set the data and always use 16-bit write operations.

Stop TM6BC counting and initialize (clear) TM6BC and RS.F.F.

TM6MD: x'00FE30'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 EN	TM6 NLD	-	-	TM6 UD1	TM6 UD0	TM6 TGE	TM6 ONE	TM6 MD1	TM6 MD0	TM6 ECLR	TM6 LP	TM6 ASEL	TM6 S2	TM6 S1	TM6 S0
0	0	-	-	0	0	0	0	0	1	0	1	0	0	1	0

(3) Set the timer 6 divisor. Since timer 6 divides TM6IOB pin input by 5, set 4 to the timer 6 compare/capture register A (TM6CA). (The valid range for TM6CA is 1 to x'FFFE'.)

TM6CA: x'00FE34'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CA15	TM6 CA14	TM6 CA13	TM6 CA12	TM6 CA11	TM6 CA10	TM6 CA9	TM6 CA8	TM6 CA7	TM6 CA6	TM6 CA5	TM6 CA4	TM6 CA3	TM6 CA2	TM6 CA1	TM6 CA0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

(4) Set the phase difference of timer 6. Since the phase difference is two cycles of prescaler 0, set 1 to the timer 6 compare/capture register B (TM6CB). (The valid range for TM6CB is -1 < TM6CB < TM6CA.)

TM6CB: x'00FE38'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CB15	TM6 CB14	TM6 CB13	TM6 CB12	TM6 CB11	TM6 CB10	TM6 CB9	TM6 CB8	TM6 CB7	TM6 CB6	TM6 CB5	TM6 CB4	TM6 CB3	TM6 CB2	TM6 CB1	TM6 CB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

TM6CAX and TM6CBX are valid only when the timer 6 compare/ capture register is set to double buffer mode.

(5) In the double buffer mode, compare TM6BC to TM6CAX. The TM6CAX is updated when TM6CAX = TM6BC, so that TM6CAX remains x'0000' before TM6BC starts counting. Therefore, to load the TM6CA value to TM6CAX, write the dummy data to TM6CAX. (The dummy data can be any values.)

TM6CAX: x'00FE36'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CAX15	TM6 CAX14	TM6 CAX13	TM6 CAX12	TM6 CAX11	TM6 CAX10	TM6 CAX9	TM6 CAX8	TM6 CAX7	TM6 CAX6	TM6 CAX5	TM6 CAX4	TM6 CAX3	TM6 CAX2	TM6 CAX1	TM6 CAX0

(6) In the double buffer mode, compare TM6BC to TM6CBX. The TM6CBX is updated when TM6CBX = TM6BC, so that TM6CBX remains x'0000' before TM6BC starts counting. Therefore, to load the TM6CA value to TM6CBX, write the dummy data to TM6CBX. (The dummy data can be any values.)

TM6CBX: x'00FE3A'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CBX15	TM6 CBX14	TM6 CBX13	TM6 CBX12	TM6 CBX11	TM6 CBX10	TM6 CBX9	TM6 CBX8	TM6 CBX7	TM6 CBX6	TM6 CBX5	TM6 CBX4	TM6 CBX3	TM6 CBX2	TM6 CBX1	TM6 CBX0

The setup steps after step (6) are the same as steps (5) and (6) in '4-3-1 Event Counter Using 16-bit Timer'.

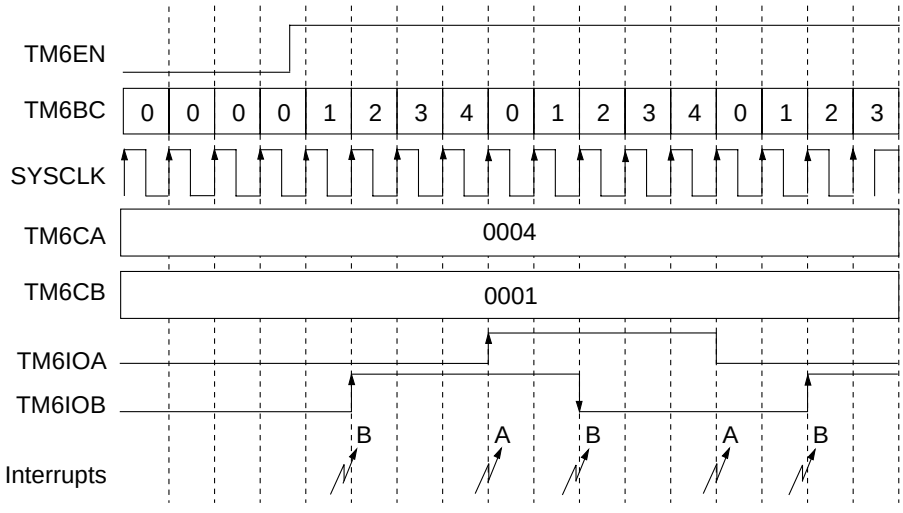


Figure 4-3-4 Two-phase PWM Timing

When timer n changes the duty of PWM output waveforms dynamically, the PWM output waveforms and interrupts may corrupt at the timing of changing the TMnCB value in the single buffer mode. In the double buffer mode, the corrupt of PWM output waveforms and interrupts does not occur at any timing of changing the TMnCB value. This corruption does not occur even when the output waveforms consist of 1 and 0.

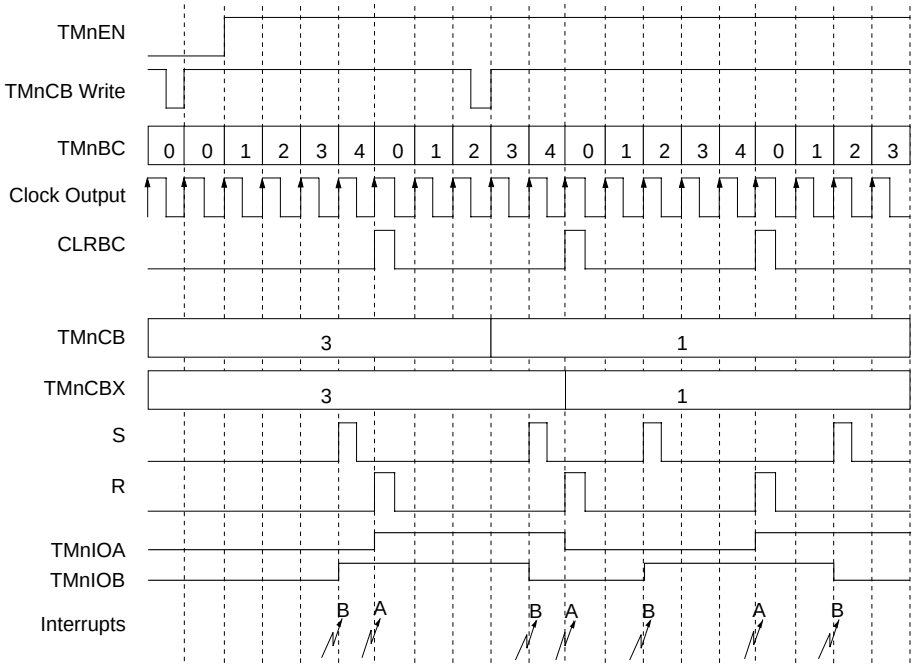


Figure 4-3-5 Two-phase PWM Timing in Double Buffer Mode

4-3-4 One-phase Capture Input Using 16-bit Timer

The one-phase capture input setup procedures for timer 6 and timer 7 are same except the up/down counting selection. In this example, timer 7 divides SYSCLK by 65536 and measures how long the TM7IOA input is high. An interrupt occurs on the capture B and the width where the TM7IOA input is high is calculated by the instruction (TMnCB - TMnCA).

Use the MOV instruction to set the data and always use 16-bit write operations.

■ Interrupt Enable Setup

(1) Enable interrupts. At the same time, clear all prior interrupt requests. Set G7LV[2:0] bits of the G7ICR to the interrupt level of 6 to 0, TM7BIR 7 and TM7BIE to 0 and 1 respectively. For example, write x'4400' to the G7ICR register. Thereafter, an interrupt occurs when the timer 7 capture B occurs.

■ Timer 7 Setup

Stop TM7BC counting and initialize (clear) TM7BC and RS.F.F.

(2) Set the operating mode to the timer 7 mode register (TM7MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Set TM7LP to 0 to count the loop of 0 to x'FFFF'. Select SYSCLK as the timer 7 clock source.

TM7MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7N LD	-	-	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	TM7 ECLR	TM7 LP	TM7 ASEL	TM7 S2	TM7 S1	TM7 S0
0	0	-	-	0	0	0	0	1	0	0	0	0	0	1	1

If this step is omitted, TM7BC may not count during the first cycle.

(3) Set TM7NLD and TM7EN of the TM7MD register to 1 and 0 respectively. This enables TM7BC, T.F.F and RS.F.F.

(4) Set both TM7NLD and TM7EN to 1. This starts the timer 7. Counting starts at the beginning of the next cycle.

■ Compare/Capture Register Setup

(5) When TM7MD[1:0] = ’10’ (the capture is selected), TM7CA and TM7CB are reserved for read operations. When setting TM7CA and TM7CB is required, first set TM7MD[1:0] to ’00’.

TM7CA: x’00FE44’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CA15	TM7 CA14	TM7 CA13	TM7 CA12	TM7 CA11	TM7 CA10	TM7 CA9	TM7 CA8	TM7 CA7	TM7 CA6	TM7 CA5	TM7 CA4	TM7 CA3	TM7 CA2	TM7 CA1	TM7 CA0

TM7CB: x’00FE48’

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CB15	TM7 CB14	TM7 CB13	TM7 CB12	TM7 CB11	TM7 CB10	TM7 CB9	TM7 CB8	TM7 CB7	TM7 CB6	TM7 CB5	TM7 CB4	TM7 CB3	TM7 CB2	TM7 CB1	TM7 CB0

TM7CA is captured on the rising edge of TM7IOA and TM7CB is captured on the falling edge of TM7IOA.

■ Interrupt Processing and Width Calculation

(6) Execute interrupt processing. The interrupt processing specifies the interrupt group and vector, and clears IRFn.

Load the TM7CA value and TM7CB value during interrupt processing.

(7) Calculate the width. Store the TM7CA value and TM7CB value to the data register and subtract TM7CA from TM7CB. Ignore C and V flags. The width is calculated correctly even though the TM7CA value is greater than the TM7CB value by setting TM7LP to 0. The following figure shows 000A - 0007 = 0003 or 3 cycles.

The width is calculated by ignoring flags even though the TM7CA value is greater than the TM7CB value.

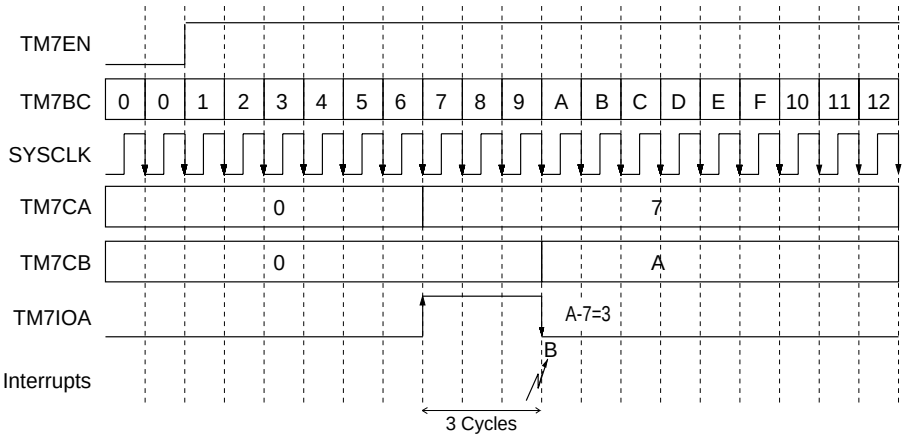


Figure 4-3-6 One-phase Capture Timing

4-3-5 Two-phase Capture Input Using 16-bit Timer

The two-phase capture input setup procedures for timer 6 and timer 7 are same except the up/down counting selection. In this example, timer 7 divides SYSCLK by 65536 and measures the width from positive edge of the TM7IOA input to the positive edge of TM7IOB input. An interrupt occurs on the capture B and the width is calculated by the instruction (TMnCB - TMnCA).

Use the MOV instruction to set the data and always use 16-bit write operations.

■ Interrupt Enable Setup

(1) Enable interrupts. At the same time, clear all prior interrupt requests. Set G7LV[2:0] bits of the G7ICR to the interrupt level of 6 to 0, TM7BIR and TM7BIE to 0 and 1 respectively. For example, write x'4400' to the G7ICR register. Thereafter, an interrupt occurs when the timer 7 capture B occurs.

■ Timer 7 Setup

Stop TM7BC counting and initialize (clear) TM7BC and RS.F.F.

(2) Set the operating mode to the timer 7 mode register (TM7MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Set TM7LP to 0 to count the loop of 0 to x'FFFF'. Select SYSCLK as the timer 7 clock source.

TM7MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7N LD	-	-	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	TM7 ECLR	TM7 LP	TM7 ASEL	TM7 S2	TM7 S1	TM7 S0
0	0	-	-	0	0	0	0	1	1	0	0	0	0	1	1

TM7CA is captured on the rising edge of TM7IOA and TM7CB is captured on the rising edge of TM7IOB.

The setup steps after step (2) are the same as steps (3) to (7) in '4-3-4 One-phase Capture Input Using 16-bit Timer'. The Figure 4-3-7 shows 000A - 0007 = 0003 or 3 cycles.

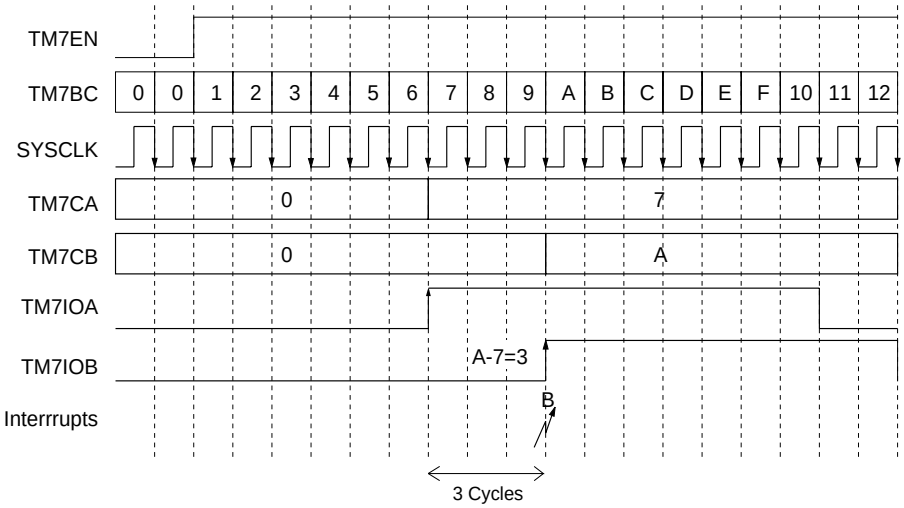


Figure 4-3-7 Two-phase Capture Timing

4-3-6 Two-phase Encoder Input Using 16-bit Timer (4x)

The two-phase encoder input setup procedures for timer 6 and timer 7 are same. In this example, timer 7 inputs the two-phase encoder (4x) and counts up/down. An interrupt occurs when the TM7BC reaches the set value.

Use the MOV instruction to set the data and always use 16-bit write operations.

■ Interrupt Enable Setup

(1) Enable interrupts. At the same time, clear all prior interrupt requests. Set G7LV[2:0] bits of the G7ICR to the interrupt level of 6 to 0, TM7BIR and TM7BIE to 0 and 1 respectively. For example, write x'4400' to the G7ICR register. Thereafter, an interrupt occurs when the timer 7 capture B occurs.

■ Timer 7 Setup

Stop TM7BC counting and initialize (clear) TM7BC and RS.F.F.

(2) Set the operating mode to the timer 7 mode register (TM7MD). Verify that counting is stopped and an interrupt is disabled. Select up counting or down counting. Set TM7LP to 1 when TM7BC starts loop counting from the TM7CA value. Set TM7LP to 0 when TM7BC counts the loop of 0 to x'FFFF'. Select two-phase encoder (4x) as the timer 7 clock source.

TM7MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7N LD	-	-	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	TM7 ECLR	TM7 LP	TM7 ASEL	TM7 S2	TM7 S1	TM7 S0
0	0	-	-	0	0	0	0	0	0	0	1	0	1	0	0

(3) Set the timer 7 looping value (the valid range is 1 to x'FFFF'). When writing x'1FFF' to TM7CA, The TM7BC counts from 0 to x'1FFF'.

TM7CA: x'00FE44'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CA15	TM7 CA14	TM7 CA13	TM7 CA12	TM7 CA11	TM7 CA10	TM7 CA9	TM7 CA8	TM7 CA7	TM7 CA6	TM7 CA5	TM7 CA4	TM7 CA3	TM7 CA2	TM7 CA1	TM7 CA0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Whenever the up or down counter reaches the TM7CA value, a compare/capture A interrupt occurs at the beginning of the next cycle.

(4) Set the value for a timer 7 interrupt when the interrupt occurs at the TM7CB value. (The valid range is 0 to TM7CA.) When the up or down counter reaches this value, a compare/capture B interrupt occurs at the beginning of the next cycle. Set the value for timer 7 interrupt when the TM7BC counts from 0 to x'FFFF'. (The valid range is 0 to x'FFFF'.)

(5) Set TM7NLD and TM7EN to 1 and 0 respectively. This enables TM7BC, T.F.F and RS.F.F. Do not change other bits of the TM7MD register.

If this step is omitted, TM7BC may not count during the first cycle.

(6) Set both TM7NLD and TM7EN to 1. This starts timer 7. Counting starts at the beginning of the next cycle.

■ Interrupt Processing

(6) Execute interrupt processing. The interrupt processing specifies the interrupt group and vector, and clears IRFn.

The following figure shows the count direction.

	Up Counting				Down Counting			
TM7IOA	↑	1	↓	0	↑	0	↓	1
TM7IOB	0	↑	1	↓	1	↑	0	↓

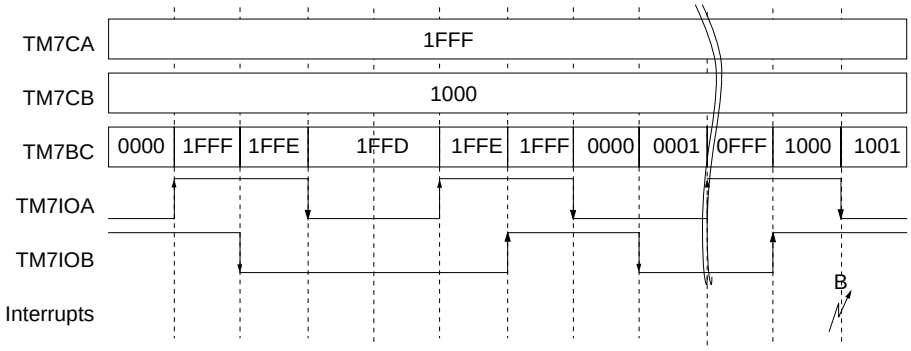


Figure 4-3-8 Two-phase Encoder Input Timing

4-3-7 One-shot Pulse Output Using 16-bit Timer

The one-shot pulse setup procedures for timer 6 and timer 7 are same. In this example, timer 7 generates a one-shot pulse. The pulse width is 2 cycles of SYSCLK.

■ Timer 7 Setup

(1) Set the operating mode to the timer 7 mode register (TM7MD). Verify that counting is stopped and an interrupt is disabled. Select up counting. Select SYSCLK as the timer 7 clock source.

Use the MOV instruction to set the data and always use 16-bit write operations.

TM7MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7N LD	-	-	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	TM7 ECLR	TM7 LP	TM7 ASEL	TM7 S2	TM7 S1	TM7 S0
0	0	-	-	0	0	0	1	0	0	0	1	0	0	1	1

Stop TM7BC counting and initialize (clear) TM7BC and RS.F.F.

(2) Set the timer 7 pulse width to TM7CA. (The valid range is 1 to x'FFFF'.) Since the timer 7 pulse width is 2 cycles of SYSCLK, write '3' to TM7CA. TM7BC counts from 0 to 3, and TM7IOA outputs high while TM7BC counts from 2 to 3.

TM7CA: x'00FE44'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CA15	TM7 CA14	TM7 CA13	TM7 CA12	TM7 CA11	TM7 CA10	TM7 CA9	TM7 CA8	TM7 CA7	TM7 CA6	TM7 CA5	TM7 CA4	TM7 CA3	TM7 CA2	TM7 CA1	TM7 CA0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

(3) Write '1' to TM7CB.

Do not output athe first one-shot pulse when TM7CB is set to '0'.

TM7CB: x'00FE48'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CB15	TM7 CB14	TM7 CB13	TM7 CB12	TM7 CB11	TM7 CB10	TM7 CB9	TM7 CB8	TM7 CB7	TM7 CB6	TM7 CB5	TM7 CB4	TM7 CB3	TM7 CB2	TM7 CB1	TM7 CB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

If this step is omitted, TM7BC may not count during the first cycle.

(4) Set TM7NLD and TM7EN to 1 and 0 respectively. This enables TM7BC, T.F.F and RS.F.F.

TM7EN is substitute for the BUSY flag for one-shot pulse.

(5) Set TM7EN to 1 when TM7IOB rises. Counting starts at the beginning of the next cycle after TM7IOB rises.

Figure 4-3-9 shows the one-shot pulse output timing. Set TM7EN on the falling edge of TM7IOB and start counting from the next cycle. Before counting starts, TM7BC is 0, the initial value of TM7IOA is 0, and a reset (R) signal and a set (S) signal cannot be output. When counting starts, TM7BC changes from 0 to 1 and the S signal is output. TM7IOA becomes 1 and the pulse is output. TM7BC reaches 3, TM7BC resets and changes from 3 to 0. At the same time, the R signal is output and TM7IOA outputs 0. Because TM7ONE is set to 1, the TM7EN flag is also reset and counting stops. When TM7IOB rises again, TM7EN is set and the same operation is repeated. As a result, the one-shot pulse is output.

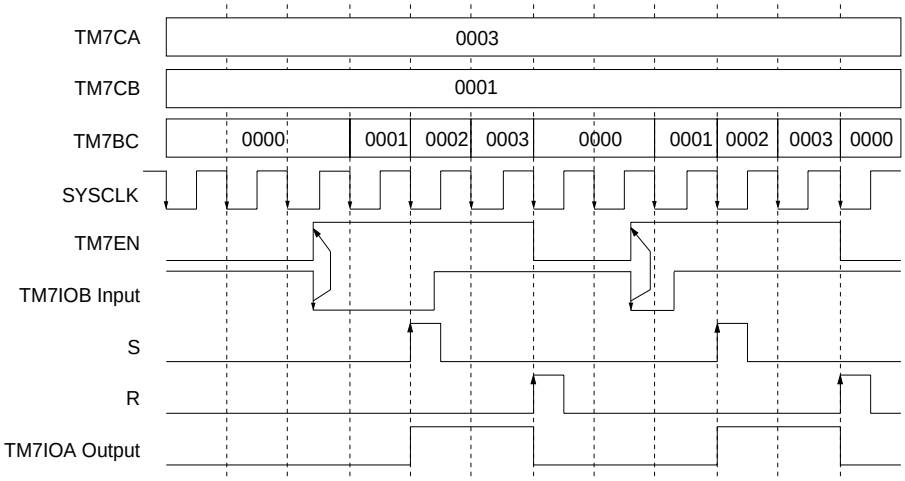


Figure 4-3-9 One-shot Pulse Output Timing

4-3-8 External Count Direction Control Using 16-bit Timer

The external count direction control setup procedures for timer 6 and timer 7 are same. In this example, timer 7 counts SYSCLK and controls the counting direction using TM7IOA. An interrupt occurs when TM7BC reaches the set value.

Use the MOV instruction to set the data and always use 16-bit write operations.

■ Interrupt Enable Setup

(1) Enable interrupts. At the same time, clear all prior interrupt requests. Set G7LV[2:0] bits of the G7ICR to the interrupt level of 6 to 0, TM7BIR and TM7BIE to 0 and 1 respectively. For example, write x'4400' to the G7ICR register. Thereafter, an interrupt occurs when the timer 7 capture B occurs.

■ Timer 7 Setup

Stop TM7BC counting and initialize (clear) TM7BC and RS.F.F.

(2) Set the operating mode to the timer 7 mode register (TM7MD). Verify that counting is stopped and an interrupt is disabled. The count direction is up when TM7IOA pin is 1 while the count direction is down when TM7IOA is 0. Select SYSCLK as the timer 7 clock source.

(3) Set the timer 7 looping value (the valid range is 1 to x'FFFF'). When writing x'1FFF' to TM7CA, The TM7BC counts from 0 to x'1FFF'. The up or down counter reaches the TM7CA value, a compare/capture A interrupt occurs at the beginning of the next cycle.

TM7MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7N LD	-	-	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	TM7 ECLR	TM7 LP	TM7 ASEL	TM7 S2	TM7 S1	TM7 S0
0	0	-	-	1	0	0	0	0	0	0	1	0	0	1	1

(4) Set the value for a timer 7 interrupt when the interrupt occurs at the TM7CB value. (The valid range is 0 to TM7CA.) When the up or down counter reaches this value, a compare/capture B interrupt occurs at the beginning of the next cycle. Set the value for timer 7 interrupt when the TM7BC counts from 0 to x'FFFF'. (The valid range is 0 to x'FFFF'.)

TM7CA: x'00FE44'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CA15	TM7 CA14	TM7 CA13	TM7 CA12	TM7 CA11	TM7 CA10	TM7 CA9	TM7 CA8	TM7 CA7	TM7 CA6	TM7 CA5	TM7 CA4	TM7 CA3	TM7 CA2	TM7 CA1	TM7 CA0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

(5) Set TM7NLD and TM7EN to 1 and 0 respectively. This enables TM7BC, T.F.F and RS.F.F. Do not change other bits of the TM7MD register.

If this step is omitted, TM7BC may not count during the first cycle.

(6) Set both TM7NLD and TM7EN to 1. This starts timer 7. Counting starts at the beginning of the next cycle.

■ Interrupt Processing

(6) Execute interrupt processing. The interrupt processing specifies the interrupt group and vector, and clears IRFn. The following figure shows the count direction.

Timer 7 controls the count direction using TM7IOA or TM7IOB. The count direction becomes the opposite edge of the count edge (shown as ❍ in Figure 4-3-10). Figure 4-3-10 shows the external count direction control timing and the example of becoming down counting from up counting and generating an interrupt.

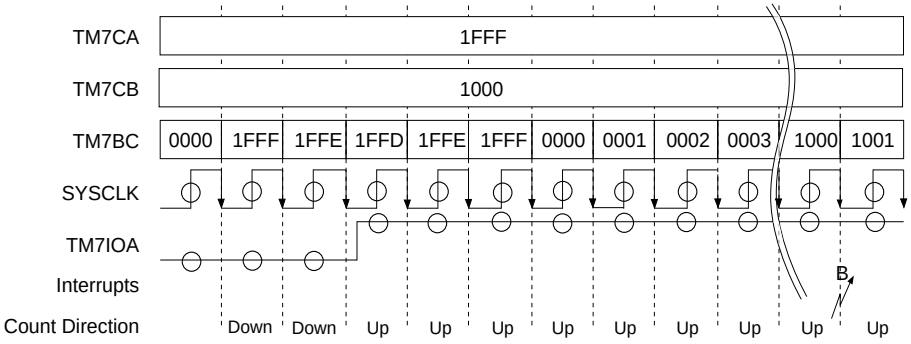


Figure 4-3-10 External Count Direction Control Timing

4-3-9 External Reset Control Using 16-bit Timer

The external reset control setup procedures for timer 6 and timer 7 are same. In this example, timer 7 is reset by an external signal while counting up.

Use the MOV instruction to set the data and always use 16-bit write operations.

■ Timer 7 Setup

(1) Set the operating mode to the timer 7 mode register (TM7MD). Verify that counting is stopped and an interrupt is disabled. Select up counting. Set TM7ECLR to 1 becuase TM7BC is reset by TM7IC pin asynchronously. Select SYSCLK as the timer 7 clock source.

Stop TM7BC counting and initialize (clear) TM7BC and RS.F.F.

TM7MD: x'00FE40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7N LD	-	-	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	TM7 ECLR	TM7 LP	TM7 ASEL	TM7 S2	TM7 S1	TM7 S0
0	0	-	-	0	0	0	0	0	0	1	1	0	0	1	1

(2) Set the timer 7 looping value (the valid range is 1 to x'FFFF'). When writing x'1FFF' to TM7CA, The TM7BC counts from 0 to x'1FFF'.

TM7CA: x'00FE44'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CA15	TM7 CA14	TM7 CA13	TM7 CA12	TM7 CA11	TM7 CA10	TM7 CA9	TM7 CA8	TM7 CA7	TM7 CA6	TM7 CA5	TM7 CA4	TM7 CA3	TM7 CA2	TM7 CA1	TM7 CA0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

If this step is omitted, TM7BC may not count during the first cycle.

(3) Set TM7NLD and TM7EN to 1 and 0 respectively. This enables TM7BC, T.F.F and RS.F.F. Do not change other bits of the TM7MD register.

(4) Set both TM7NLD and TM7EN to 1. This starts timer 7. Counting starts at the beginning of the next cycle.

Thereafter, timer 7 is reset asynchronously when TM7IC is high. This allows external synchronization easily. It can be used to adjust the motor or to initialize the timer by hardware.

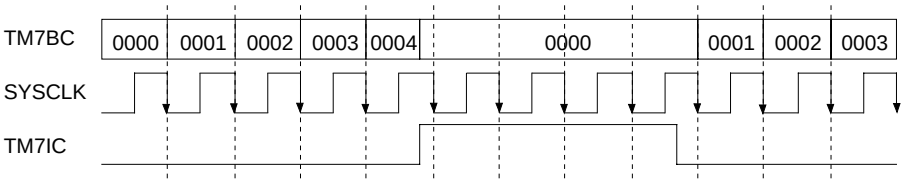


Figure 4-3-11 External Reset Control Timing

Chapter 5 Serial Interface

5

5-1 Serial Interface

5-1-1 Overview

This LSI series contains two serial interfaces. Each serial interface transmits and receives the data in the synchronous mode, asynchronous mode and I²C mode. The maximum baud speed in synchronous mode is SYSCLK/4. The maximum baud speed in asynchronous mode is 312,500 bps with a 20-MHz oscillator. (The baud speed can be set to 312,500 bps or more by changing the oscillation frequency.)

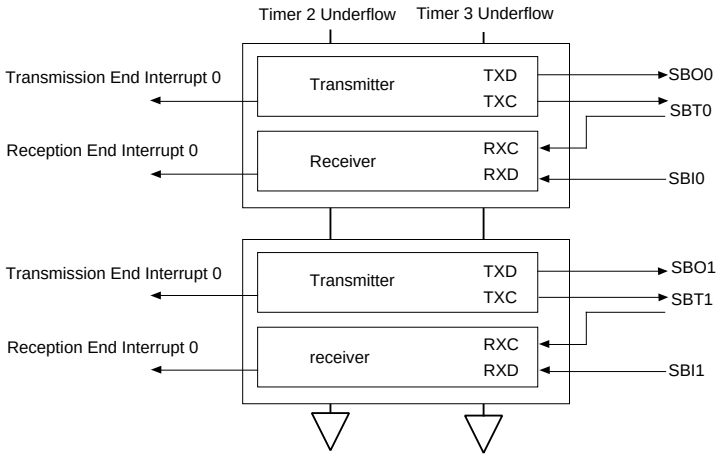


Figure 5-1-1 Serial Interface Configuration

Table 5-1-1 Serial Interface Features

	Synchronous Serial Interface	Asynchronous Serial Interface	I²C
Parity	None, 0, 1, Even, Odd		—
Character Length	7-bit, 8-bit		8-bit
Bit Order	LSB first, MSB first	LSB	MSB
Clock Source	Timer 2/16 or Timer 3/16 External Clock Timer 2/2 (Ch0) Timer 3/2 (Ch1)	Timer 2/16 or Timer 3/16	Timer 2/16 or Timer 3/16
Max. Transfer Speed	2,500,000 bps (with a 20-MHz Oscillator)	312,500 bps (with a 20-MHz Oscillator)	100,000 bps
Error Detect	Parity Error Overrun Error	Parity Error Overrun Error Framing Error	Slave Response
Buffer	Independent Transmit/Receive buffer (Single Transmit Buffer, Double Receive		←
Interrupt	Transmission End Interrupt, Reception End Interrupt		←

5-1-2 Control Registers

Three registers control the serial interface: serial control register (SCnCTR), serial transmit/receive register (SCnTRB) and serial status register (SCnSTR).

Table 5-1-2 List of Serial Interface Control registers

	Serial Interface 0	Serial Interface 1
Serial Control Register	Serial 0 Control Register (SC0CTR), x'00FD80'	Serial 1 Control Register (SC1CTR), x'00FD90'
Serial Transmit/Receive Register	Serial 0 Transmit/Receive Register (SC0TRB), x'00FD82'	Serial 1 Transmit/Receive Register (SC1TRB), x'00FD92'
Serial Status Register	Serial 0 Status Register (SC0STR), x'00FD83'	Serial 1 Status Register (SC1STR), x'00FD93'

The serial control register (SCnCTR) sets the operating conditions for serial interface. This register controls clock source selection, parity bit selection, protocol selection and transmit/receive enable.

The transmit data is written to the serial transmit/receive register (SCnTRB), while the receive data is written to the SCnTRB register. The transmission starts at the end of the first cycle or second cycle of the transfer clock (timer 2 underflow or timer 3 udnerflow) after the data is written to SCnTRB. The serial transmission is operated in double buffer mode. After the reception is completed, the data is set to the SCnTRB register. The receive data is loaded when an interrupt occurs or the SCnRXA flag of the SCnSTR register is 1.

The serial status register (SCnSTR) reads the status of error detection of serial interface. An overrun error occurs when the next data is received before the received data is loaded by SCnTRB. An error does not occur on the next cycle by reading the SCnTRB register. The overrun error data is updated when the last bit (the 7th bit or the 8th bit) of the data is received. A parity error occurs when the parity bit is 1 although it is supposed to 0, when the parity bit is 0 although it is supposed to 1, when the parity bit is odd although it is even and when the parity bit is even although it is supposed to set odd. The parity error data is updated when the parity bit is received. A framing error occurs when the stop bit is 0. The framing error data is updated when the stop bit is received. Figure 5-1-2 shows the timing when each bit of the serial status register (SCnSTR).

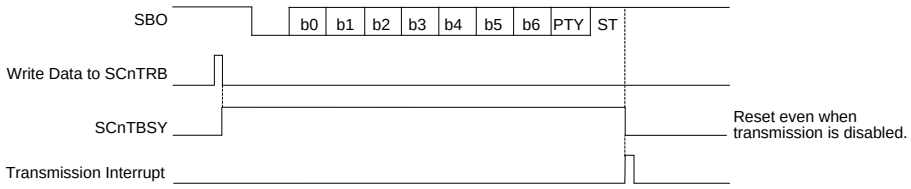
Igonore MSB (bit 7) in the 7-bit transmission.

Write the data to the serial transmit/receive register after verifying the data is not in transmission by checking the SCnTBSY of the SCnSTR register or a transmission end interrupt. The serial transmission may not occur if writing to the serial transmit/receive register during the transmission is operated.

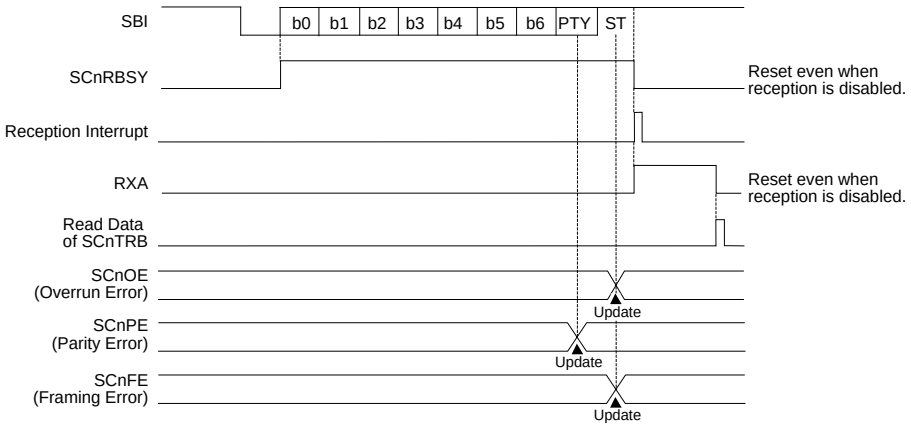
The MSB (bit 7) becomes 0 in the 7-bit reception.

■ Asynchronous/Synchronous Timing

Transmission



Reception



■ I^2C Timing

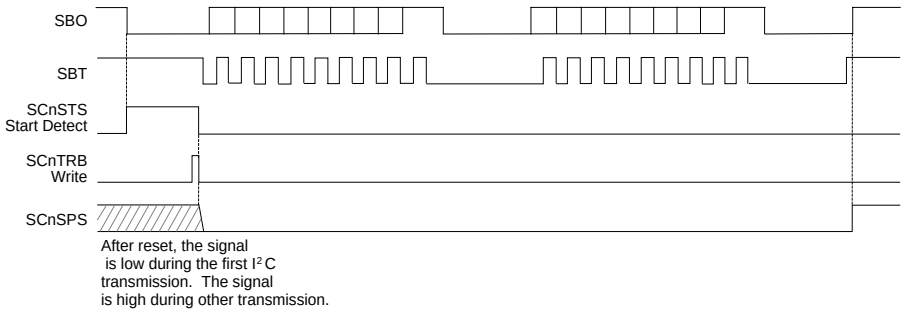

SBO
SBT
SCnSTS Start Detect
SCnTRB Write
SCnSPS
After reset, the signal is low during the first I²C transmission. The signal is high during other transmission.

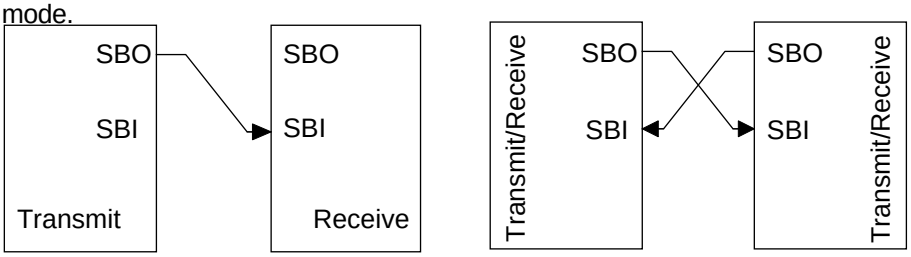
Figure 5-1-2 SCnSTR Change Timing

5-1-3 Serial Interface Connection

There are six serial interface connecting methods.

■ Asynchronous Mode

The serial interface can connect using either simplex transfer or duplex transfer mode.

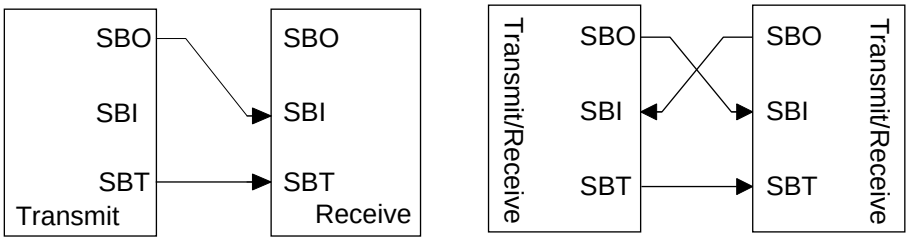


Simplex Connection　　Duplex Connection

Figure 5-1-3 Asynchronous Connection

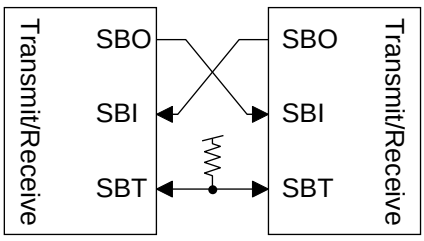
■ Synchronous Mode

The serial interface can connect using either simplex transfer, duplex transfer or half-duplex transfer mode.



Simplex Connection　　Duplex Connection

See 'Chapter 7' for SBT port setup.



Half-duplex Connection

Figure 5-1-4 Synchronous Connection

When the data cannot be transmitted in half-duplex mode, both SBT pins become input so that they need pull-up resistors. The SBT pins connect a pull-up resistor externally or a built-in pull-up resistor by the PPLU register.

The I²C mode is used only as the master transmission/reception in the single master system. Because I²C mode do not control the protocol, setting the transfer baud rate and controlling the transfer start are required to function the slave transmission/reception.

■ I²C Mode

The serial interface can connect to the devices which can slave transmit and receive. The SBO pin and SBT pin connect pull-up resistors (externally or internally).

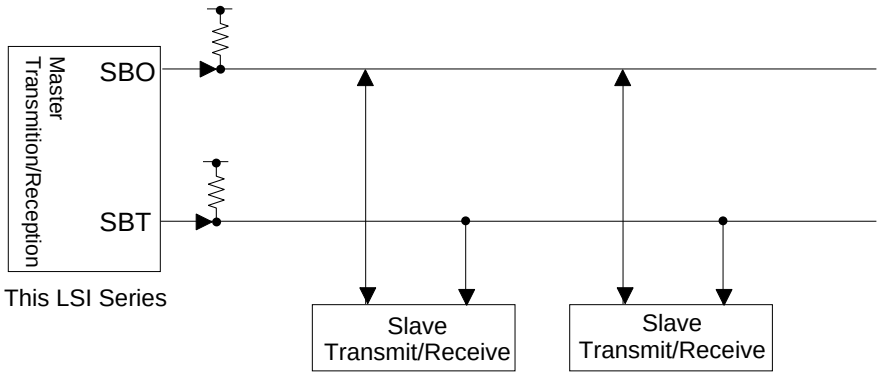


Figure 5-1-5 I²C Mode Connection

The acknowledge (ACK) bit is substituted for a parity bit. In the system requiring the ACK, fix the parity bit to 1 (SCnPTY[2:0] = 101) when this LSI master transmits the data. In that case, a parity error occurs when the ACK (low level) returns from the slave. Therefore, the parity bit of the SCnSTR register becomes 1 when the transmission is completed normally.
On the other hand, when this LSI master receives the data, fix the parity bit to 0 (SCnPTY[2:0] = 100) if the ACK returns from the slave and set the parity bit to 1 (SCnPTY[2:0] = 101) if the ACK does not return.

During I²C transmission/reception, the transmit state flag of the SCnSTR register shows the transmission/reception in progress.

■ Asynchronous Serial Transfer Speed

In asynchronous mode, set the serial transfer clock to 16 times of transfer baud rate. The following is the baud rate calculation.

Baud Rate (bps) = OSCI, OSCO x 1/32 x 1/timer divisor

The transmission is possible if the baud rate error is within 2 %. Table 5-1-3 to Table 5-1-10 show the baud rates with frequently used oscillators.

Table 5-1-3 Baud Rate Setup Example in Asynchronous Mode

External Oscillator at 20 MHz				
Baud Rate	Divisor	Real Time	Error	
1200	520 *	1201.92	0.16	
2400	260 *	2403.85	0.16	
4800	130	4807.69	0.16	
9600	65	9615.38	0.16	
19200	33	18939.39	-1.36	
28800	22	28409.09	-1.36	
31250	20	31250.00	0.00	
38400	16	39062.50	1.73	
48000	13	48076.92	0.16	
57600	11	56818.18	-1.36	
76800	8	78125.00	1.73	
153600	4	156250.00	1.73	
307200	2	312500.00	1.73	
312500	2	312500.00	0.00	(Max)

* : Available with Timer 0 in case of the divisor of 256 or greater.

Table 5-1-4 Baud Rate Setup Example in Asynchronous Mode

External Oscillator at 19.6608 MHz				
Baud Rate	Divisor	Real Time	Error	
1200	520 *	1181.54	-1.54	
2400	260 *	2363.08	-1.54	
4800	130	4726.15	-1.54	
9600	65	9452.31	-1.54	
19200	32	19200.00	0.00	
28800	21	29257.14	1.59	
31250	20	30720.00	-1.70	
38400	16	38400.00	0.00	
48000	13	47261.54	-1.54	
57600	11	55854.55	-3.03	
76800	8	76800.00	0.00	
153600	4	153600.00	0.00	
307200	2	307200.00	0.00	(Max)

* : Available with Timer 0 in case of the divisor of 256 or greater.

Table 5-1-5 Baud Rate Setup Example in Asynchronous Mode

External Oscillator at 17.2032 MHz				
Baud Rate	Divisor	Real Time	Error	
1200	448 *	1200.00	0.00	
2400	224	2400.00	0.00	
4800	112	4800.00	0.00	
9600	56	9600.00	0.00	
19200	28	19200.00	0.00	
28800	19	28294.74	-1.75	
31250	17	31623.53	1.20	
38400	14	38400.00	0.00	
48000	11	48872.73	1.82	
57600	9	59733.33	3.70	
76800	7	76800.00	0.00	
153600	3	179200.00	16.67	
268800	2	268800.00	0.00	(Max)

* : Available with Timer 0 in case of the divisor of 256 or greater.

Table 5-1-6 Baud Rate Setup Example in Asynchronous Mode

External Oscillator at 16 MHz				
Baud Rate	Divisor	Real Time	Error	
1200	417 *	1199.04	-0.08	
2400	208	2403.85	0.16	
4800	104	4807.69	0.16	
9600	52	9615.38	0.16	
19200	26	19230.77	0.16	
28800	17	29411.76	2.12	
31250	16	31250.00	0.00	
38400	13	38461.54	0.16	
48000	10	50000.00	4.17	
57600	9	55555.56	-3.55	
76800	7	71428.57	-6.99	
153600	3	166666.67	8.51	
250000	2	250000.00	0.00	(Max)

* : Available with Timer 0 in case of the divisor of 256 or greater.

Table 5-1-7 Baud Rate Setup Example in Asynchronous Mode

External Oscillator at 14 MHz				
Baud Rate	Divisor	Real Time	Error	
1200	368 *	1188.86	-0.93	
2400	184	2377.72	-0.93	
4800	92	4755.43	-0.93	
9600	46	9510.87	-0.93	
19200	23	19021.74	-0.93	
28800	15	29166.67	1.27	
31250	14	31250.00	0.00	
38400	11	39772.73	3.57	
48000	9	48611.11	1.27	
57600	8	54687.50	-5.06	
76800	6	72916.67	-5.06	
153600	3	145833.33	-5.06	
218750	2	218750.00	0.00	(Max)

* : Available with Timer 0 in case of the divisor of 256 or greater.

Table 5-1-8 Baud Rate Setup Example in Asynchronous Mode

External Oscillator at 12 MHz				
Baud Rate	Divisor	Real Time	Error	
1200	312 *	1201.92	0.16	
2400	156	2403.85	0.16	
4800	78	4807.69	0.16	
9600	39	9615.38	0.16	
19200	20	18750.00	-2.34	
28800	13	28846.15	0.16	
31250	12	31250.00	0.00	
38400	10	37500.00	-2.34	
48000	8	46875.00	-2.34	
57600	7	53571.43	-6.99	
76800	5	75000.00	-2.34	
153600	3	125000.00	-18.62	
187500	2	187500.00	0.00	(Max)

* : Available with Timer 0 in case of the divisor of 256 or greater.

Table 5-1-9 Baud Rate Setup Example in Asynchronous Mode

External Oscillator at 10 MHz				
Baud Rate	Divisor	Real Time	Error	
1200	260 *	1201.92	0.16	
2400	130	2403.85	0.16	
4800	65	4807.69	0.16	
9600	33	9469.70	-1.36	
19200	16	19531.25	1.73	
28800	11	28409.09	-1.36	
31250	10	31250.00	0.00	
38400	8	39062.50	1.73	
48000	7	44642.86	-6.99	
57600	5	62500.00	8.51	
76800	4	78125.00	1.73	
153600	2	156250.00	1.73	
156250	2	156250.00	0.00	(Max)

* : Available with Timer 0 in case of the divisor of 256 or greater.

Table 5-1-10 Baud Rate Setup Example in Asynchronous Mode

External Oscillator at 8 MHz				
Baud Rate	Divisor	Real Time	Error	
1200	208	1201.92	0.16	
2400	104	2403.85	0.16	
4800	52	4807.69	0.16	
9600	26	9615.38	0.16	
19200	13	19230.77	0.16	
28800	9	27777.78	-3.55	
31250	8	31250.00	0.00	
38400	7	35714.29	-6.99	
48000	5	50000.00	4.17	
57600	4	62500.00	8.51	
76800	3	83333.33	8.51	
125000	2	125000.00	0.00	(Max)

5-2 Serial Interface Setup Examples

5-2-1 Serial Transmission in Asynchronous Mode Using Timer 2

This section describes the example of serial interface 0 transmission ■ asynchronous mode with the following settings:

- 20 MHz oscillation
- Baud Rate = 9600 bps (SYSCLK/65 by timer 2)
- Bit Order: LSB
- 8-bit data transfer
- Two stop bits
- Odd parity

The next data is transmitted when a transmission end interrupt occurs.

Figure 5-2-1 Aynchronous Transmission Configuration

The transmission starts when the data is written to the SC0TRB register. The transmission starts synchronizing with timer 2 underflow. An interrupt occurs after the transmission is completed and the new data is written to the SC0TRB register during the interrupt service routine. The SC0TBSY flag of the SC0STR register polls if an interrupt does not occur.

Setting timer is required during serial reception in asynchronous mode.

The serial interface generates the serial transfer baud rate with timer 2 or timer 3 divided by 16. With a 20-MHz oscillator (SYSCLK is 10 MHz) and 9600 bps, 10 MHz/16/9600 = 65.10
Therefore, set the timer 2 or timer 3 underflow to 65.

■ Pin Setup

Set P72 pin to data output of serial interface 0. [See Chapter 8 Ports]

■ Timer 2 Setup

(1) Verify that counting is stopped with the timer 2 mode register (TM2MD).

This verification is unnecessary immediately after a reset.

TM2MD: x'00FE22'

7	6	5	4	3	2	1	0
TM2 EN	TM2 LD	-	-	-	-	TM2 S1	TM2 S0
0	0	-	-	-	-	1	1

(2) Set the timer 2 divisor. Since the timer 2 divisor is SYSCLK/65, set the timer 2 base register (TM2BR) to 64. (The valid range is 1 to 255.)

TM2BR: x'00FE12'

7	6	5	4	3	2	1	0
TM2 BR7	TM2 BR6	TM2 BR5	TM2 BR4	TM2 BR3	TM2 BR2	TM2 BR1	TM2 BR0
0	1	0	0	0	0	0	0

(3) Load the TM2BR value to TM2BC. To do this, set TM2LD and TM2EN to 1 and 0 respectively. At the same time, select the clock source.

Do not change the clock source once you have selected it. Changing the clock source while controlling count operation will corrupt the binary counter value.

(4) Set both TM2LD and TM2EN to 0.

If this step is omitted, TM2BC may not count during the first cycle.

(5) Set TM2LD and TM2EN to 0 and 1 respectively. This starts timer 2.

■ Serial Interface 0 Setup

(6) Enable interrupts. At this point, clear all prior interrupt requests. Set the G3ICR register to the interrupt level (level 6 to 0), SC0TIR and SC0TIE to 0 and 1 respectively. For example, write the G3ICR register to xÕ4400Õ. Thereafter, a serial transmission end interrupt occurs when the data written to the serial transmit/receive register is transferred.

G3ICR: x'00FC46'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G3 LV2	G3 LV1	G3 LV0	SC0R IE	SC0T IE	TM2 IE	IRQ2 IE	SC0R IR	SC0T IR	TM2 IR	IRQ2 IR	SC0R ID	SC0T ID	TM2 ID	IRQ2 ID
0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

(7) Set the operating control conditions to the serial 0 control register (SC0CTR). Set asynchronous mode, LSB for bit order, timer 2/16, 8-bit data transfer, 2 stop bits and odd parity.

SC0CTR: x'00FD80'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC0 TEN	SC0 REN	SC0 BRE	SC0 I2CS	SC0 PTL	-	SC0 OD	SC0 I2CM	SC0 LN	SC0 PTY2	SC0 PTY1	SC0 PTY0	SC0 SB	SC0 POD	SC0 S1	SC0 S0
1	1	0	0	0	-	0	0	1	1	1	1	1	0	0	1

(8) Set the first data to be transferred to the serial 0 transmit/receive register (SC0TRB). When the data to be transferred is set to the SC0TRB register, the transmission starts synchronizing with timer 2. Execute the interrupt service routine and transfer the next data when an interrupt occurs.

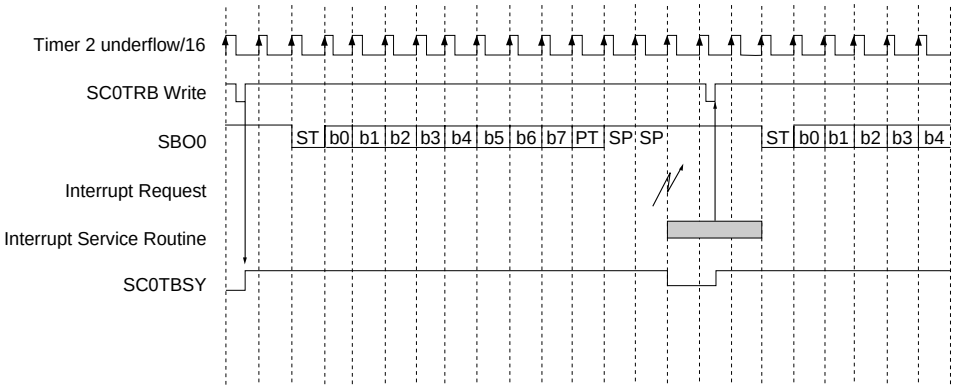


Figure 5-2-2 Bit Transmission Timing in Asynchronous Mode

5-2-2 Serial Reception in Synchronous Mode Using Timer 2

This section describes the example of serial interface 0 reception in synchronous mode with the following settings:

- Bit Order: MSB
- 8-bit data transfer
- Even parity

The next data is read when a reception end interrupt occurs.

■ Pin Setup

Set P70 pin and P71 pin to serial clock input and data input of serial interface 0 respectively. [See Chapter 8 Ports]

■ Serial Interface 0 Setup

(1) Set the operating control conditions to the serial 0 control register (SC0CTR). Set synchronous mode, MSB for bit order, the external clock source, 8-bit data transfer and even parity.

SC0CTR: x'00FD80'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC0 TEN	SC0 REN	SC0 BRE	SC0 I2CS	SC0 PTL	-	SC0 OD	SC0 I2CM	SC0 LN	SC0 PTY2	SC0 PTY1	SC0 PTY0	SC0 SB	SC0 POD	SC0 S1	SC0 S0
1	1	0	0	1	-	1	0	1	1	1	0	0	0	0	0

(2) Enable interrupts. At this point, clear all prior interrupt requests. Set the G3ICR register to the interrupt level (level 6 to 0), SC0RIR and SC0RIE to 0 and 1 respectively. For example, write the G3ICR register to xÕ4800Õ. Thereafter, a serial reception end interrupt occurs when the data is transferred to the serial transmit/receive register.

G3ICR: x'00FC46'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G3 LV2	G3 LV1	G3 LV0	SC0R IE	SC0T IE	TM2 IE	IRQ2 IE	SC0R IR	SC0T IR	TM2 IR	IRQ2 IR	SC0R ID	SC0T ID	TM2 ID	IRQ2 ID
0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0

After specifying the interrupt group and vector, and clearing IRFn, program the interrupt service routine.

Thereafter, an interrupt occurs when the serial data is received.

5-2-3 Serial Transmission/Reception in I²C Mode Using Timer 3

This section describes the example of serial interface 0 transmission/reception in I²C mode explaining I²C start sequence transmission, data transmission, data reception and I²C stop sequence transmission in order.

■ Pin Setup

Set P70 pin and P72 pin to serial clock input and port input respectively. If P70 pin and P72 pin do not equip a pull-up resistor externally, set the pull-up resistor by the pull-up control register. [See Chapter 8 Ports]

When selecting P70 and P72 to I²C mode by the serial 0 control register, these pins becomes output mode. Therefore, they should be set to input when they are used as ports.

■ Serial Interface 0 Setup

<Initial Setup>

(1) Set the operating conditions to the serial 0 control register (SC0CTR). In I²C mode, select open-drain, 8-bit data transfer, MSB as the bit order. In the system with the response from slave (ACK), set parity bit to 1. (In the system without ACK, select no parity.) Select timer 3 underflow/16 as the clock source.

In this example, select the slave response.

SC0CTR: x'00FD80'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC0 TEN	SC0 REN	SC0 BRE	SC0 I2CS	SC0 PTL	-	SC0 OD	SC0 I2CM	SC0 LN	SC0 PTY2	SC0 PTY1	SC0 PTY0	SC0 SB	SC0 POD	SC0 S1	SC0 S0
1	1	0	0	1	-	1	1	1	1	0	1	0	1	1	1

Set both the transmission enable flag and the reception enable flag to 1.

<Start Sequence>

(2) Set the I²C sequence output bit of the serial 0 control register (SC0CTR) to 1. This makes the SBO pin output low and generates the start sequence.

SC0CTR: x'00FD80'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC0 TEN	SC0 REN	SC0 BRE	SC0 I2CS	SC0 PTL	-	SC0 OD	SC0 I2CM	SC0 LN	SC0 PTY2	SC0 PTY1	SC0 PTY0	SC0 SB	SC0 POD	SC0 S1	SC0 S0
1	1	0	1	1	-	1	1	1	1	0	1	0	1	1	1

<Data Transmission>

(3) Load the data to the serial 0 transmit/receive register. This allows the data to output. The SBO pin output changes with 1/8 cycles delay of the falling edge of the SBT pin output.

After transmission, both SBO pin output and SBT pin output stay low.

(4) After transmission ends, read the dummy data of the serial 0 transmit/ receive register (SC0TRB).

An interrupt (a serial 0 transmission end interrupt or a serial 0 reception end interrupt) or polling the serial status register identifies the transmission end.

(Polling the reception state flag during I²C mode is prohibited.)

(5) Read the serial 0 status register and verify the parity error. If a parity error occurs, the response is obtained from the slave correctly. If a parity error does not occur, the response is not obtained from the slave. (This step is not required in the system without ACK.)

When the data is transmitted continuously, repeat the steps (3) to (5).

<Data Reception>

(6) Load the dummy data x'FF' to the serial 0 transmit/receive register (SC0TRB). This allows the SBO pin to output resistive high (because the SBO pin is an open-drain pin) and input low when the slave outputs low.

An interrupt (a serial 0 transmission end interrupt or a serial 0 reception end interrupt) or polling the serial status register identifies the reception end.

(Polling the reception state flag during I²C mode is prohibited.)

(7) After reception ends, retrieve the received data by reading the serial 0 transmit/receive register (SC0TRB).

When the data is received continuously, repeat the steps (6) and (7).

<Stop Sequence>

(8) Set the I²C sequence output bit of the serial 0 control register (SC0CTR) to 0. This makes the SBT pin output high and generates the stop sequence.

SC0CTR: x'00FD80'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC0 TEN	SC0 REN	SC0 BRE	SC0 I2CS	SC0 PTL	-	SC0 OD	SC0 I2CM	SC0 LN	SC0 PTY2	SC0 PTY1	SC0 PTY0	SC0 SB	SC0 POD	SC0 S1	SC0 S0
1	1	0	0	1	-	1	1	1	1	0	1	0	1	0	1

(9) Disable the reception enable flag once immediately after the stop sequence is generated.

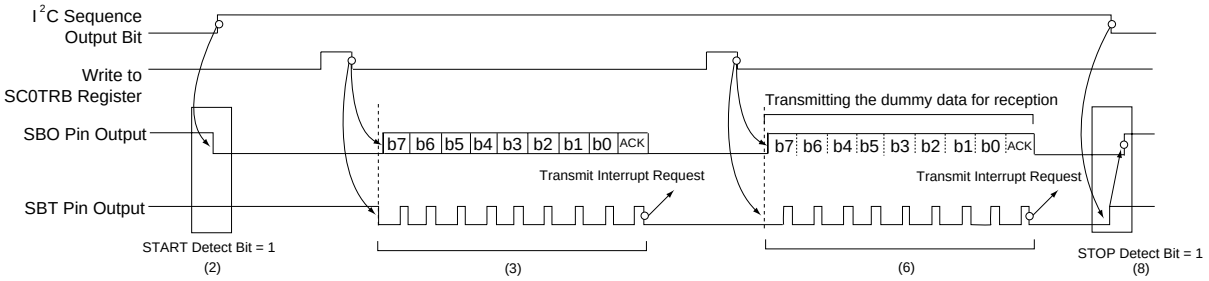


Figure 5-2-3 Transmission/Reception in I²C Mode

Chapter 6 Analog Interface

6

6-1 Analog Interface

6-1-1 Overview

This LSI series contains a 8-bit charge redistribution A/D converter. The A/D converter supports digital signal processing in the voice and audio frequency ranges with a 8-bit resolution, a maximum conversion frequency of 208 kHz (4.8 µs per channel with a 20-MHz oscillator) and a low current.

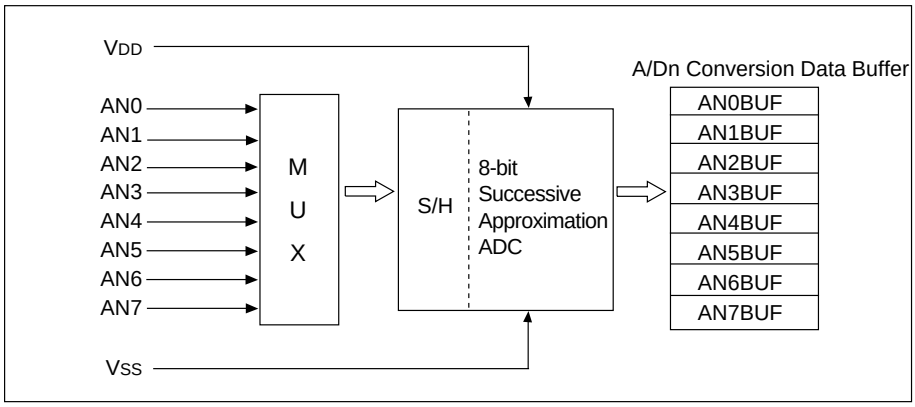


Figure 6-1-1 Analog Interface Configuration

■ Notices When Using A/D Converter

(1) Set the impedance of the analog signal for A/D conversion to 8 kΩ or less.

(2) Connect the A/D input pin to the condenser of 2000 pF or more to control the voltage change of the A/D input pin if the impedance of the analog signal cannot be set to 8 kΩ or less.

(3) To prevent the power potential fluctuation, do not change the chip output level from high level to low level or vice verse, or do not switch the peripheral load circuit on/off during A/D conversion.

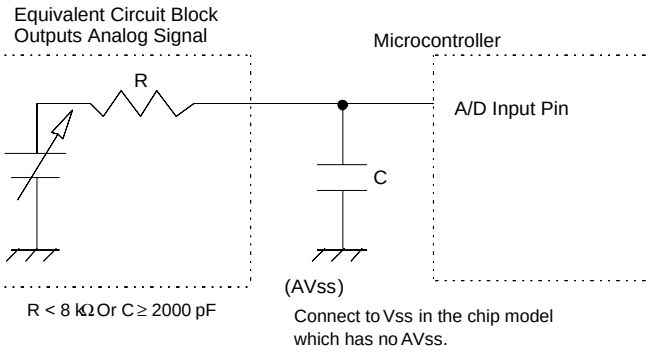


Table 6-1-1 A/D Converter Functions

Feature	Description
S/H	Built-in
Conversion Resolution	8-bit ± 3 LSB (AN3 to AN0) 8-bit ± 4 LSB (AN7 to AN4) The A/D converter converts the voltage between VDD and Vss divided into 256 and this converted result is tored in AN7BUF to AN0BUF.
Conversion Time	4.8 µs or more per channel (sample time of 400 ns with a 20-MHz oscillator)
Clock Source	Internal System Clock SYSCLK divided by 1, 2, 4, 8
Operating Mode	30 operating modes: Single conversion of single channel (channel 0 to channel 7) Single conversion of multiple channels (channel 0 to channel 1, channel o to channel 2, channel 0 to channel 3, channel 0 to channel 4, channel 0 to channel 5, channel 0 to channel 6, channel 0 to channel 7) Continuous conversion of single channel (channel 0 to channel 7) Continuous conversion of multiple channels (channel 0 to channel 1, channel o to channel 2, channel 0 to channel 3, channel 0 to channel 4, channel 0 to channel 5, channel 0 to channel 6, channel 0 to channel 7)
Conversion Start	Timer 1 underflow or register setting
Interrupt	An interrupt occurs each time the conversion sequence ends.

'Ch' stands for channel. ANn pin corresponds to the channel number. For example, the AN3 pin corresponds to channel 3.

■ Selecting the A/D Converter Clock Source

The A/D converter clock source is selected to SYSCLK, SYSCLK/2, SYSCLK/4 or SYSCLK/8 as the conversion time is 4.8 µs or more. Select the A/D converter clock source as follows:

SYSCLK frequency/divisor $\leq$ 5 MHz

For example, select the A/D converter clock source as SYSCLK/4 (the conversion speed of 4.8 µs) or SYSCLK/8 (the conversion time of 9.6 µs) with a 20-MHz oscillator. Select SYSCLK/2, SYSCLK/4 or SYSCLK/8 with a 10-MHz oscillator. Select SYSCLK. SYSCLK/2, SYSCLK/4, SYSCLK/8 with a 5-MHz oscillator or less. The conversion time is 12 cycles of the A/D converter clock source as Figure 6-1-2 shows. For example, the conversion time is calculated as follows when SYSCLK/4 is selected.

[SYSCLK cycle (s) $\times$ 4 (divisor) $\times$ 12 (cycle)]

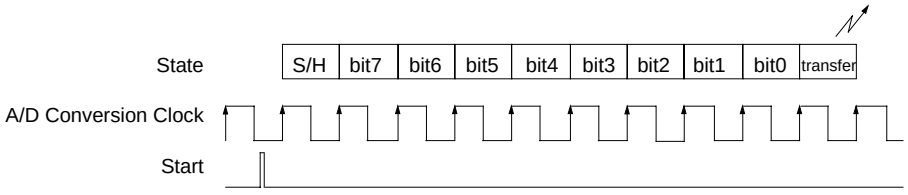


Figure 6-1-2 A/D Conversion Timing

■ One Channel/Single Conversion

The A/D converter converts one A/D input signal of 1 channel once. An interrupt occurs as soon as the conversion ends. Set the channel to be converted to AN1CH[2:0] bits. Set the ANTM1 flag and the ANEN flag to 0 and 1 respectively when the conversion starts using the ANEN flag. The ANEN flag becomes 1 during the conversion and 0 when the conversion ends.

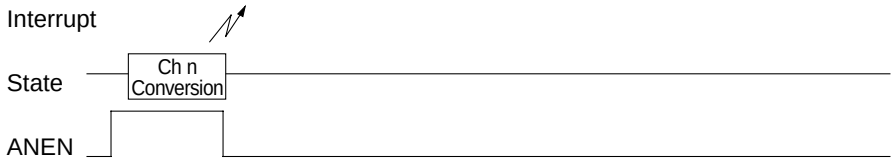


Figure 6-1-3 One Channel/Single Conversion Timing

■ Multiple Channels/Single Conversion

The A/D converter converts A/D input signals of continuous channels from channel 0 once. An interrupt occurs as soon as the conversion for all channels ends. Set AN1CH[2:0] bits to channel 0 and the ANNCH flag to the last channel to be converted. Set the ANTM1 flag and the ANEN flag to 0 and 1 respectively when the conversion starts using the ANEN flag. The ANEN flag becomes 1 during the conversion and 0 when the conversion sequence ends. In addition, the AN1CH[2:0] bits are set to the channel number during the conversion and channel 0 after the conversion sequence ends.

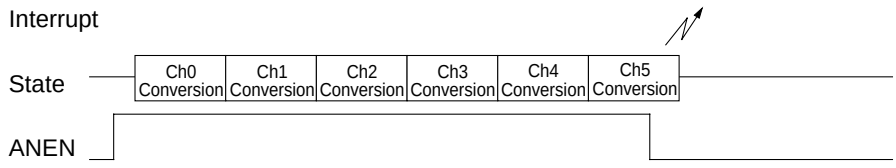


Figure 6-1-4 Multiple Channels/Single Conversion Timing

■ One Channel/Continuous Conversion

The A/D converter converts one A/D input signal continuously. An interrupt occurs each time the conversion ends. Set AN1CH[2:0] bits to the channel number to be converted. Set the ANTM1 flag and the ANEN flag to 0 and 1 respectively when the conversion starts using the ANEN flag. Setting the ANEN flag to 0 ends the conversion forcibly.

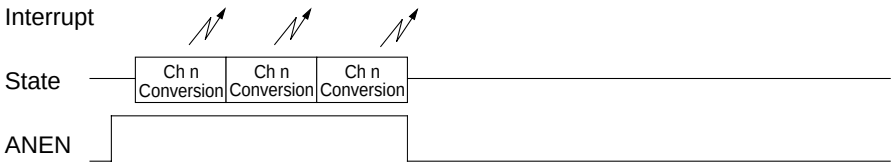


Figure 6-1-5 One Channel/Continuous Conversion Timing

■ Multiple Channels/Continuous Conversion

The A/D converter converts A/D input signals of continuous channels from channel 0 continuously. An interrupt occurs each time the continuous conversion ends. Set AN1CH[2:0] bits to channel 0 and the ANNCH flag to the last channel to be converted. (The conversion starts from channel 0.) Set the ANTM1 flag and the ANEN flag to 0 and 1 respectively when the conversion starts using the ANEN flag. The ANEN flag becomes 1 during the conversion and 0 when the conversion sequence ends. Setting the ANEN flag to 0 ends the conversion forcibly. The AN1CH[2:0] bits are set to the channel number during the conversion and channel 0 after the conversion sequence ends.

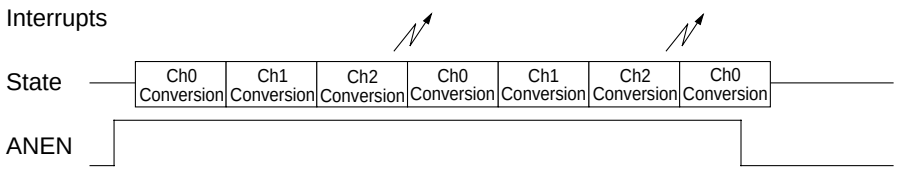


Figure 6-1-6 Multiple Channels/Continuous Conversion Timing

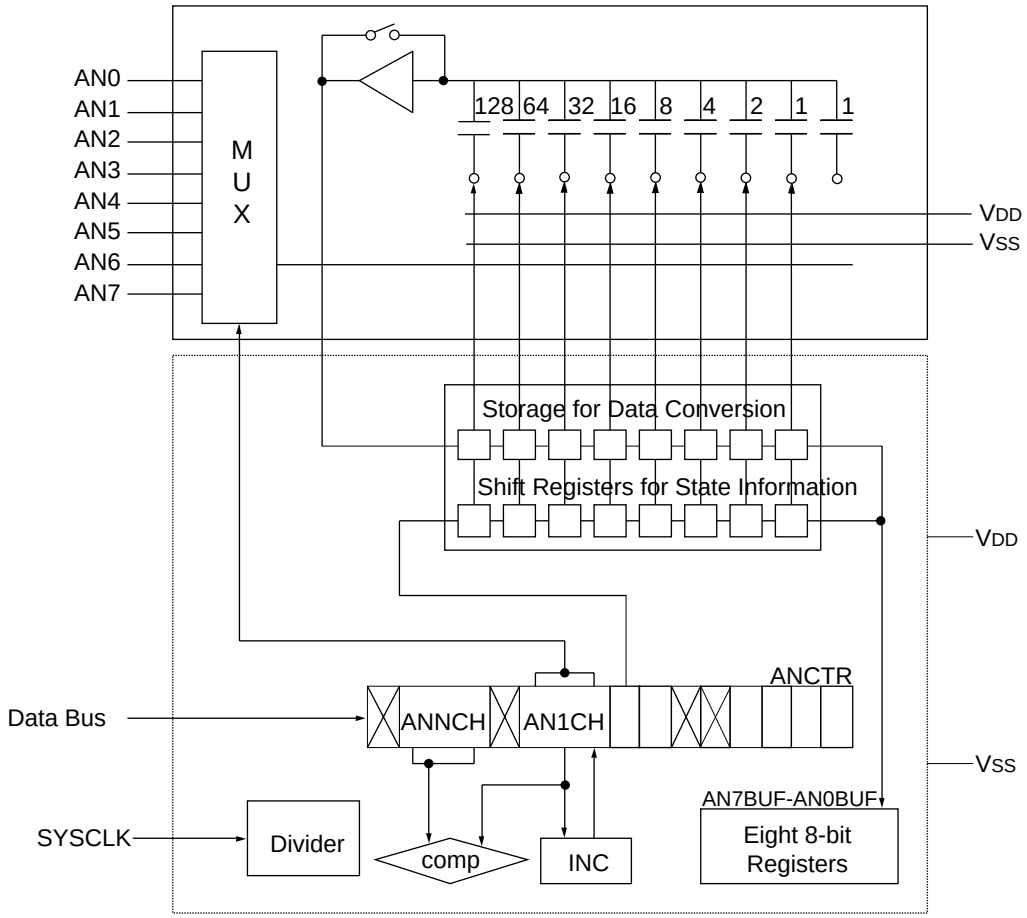


Figure 6-1-7 Analog Interface Block Diagram

6-1-2 Control Registers

The A/D converter contains the A/D conversion control register (ANCTR) and the A/D conversion data buffers (ANnBUF) corresponding to channel 7 to channel 0 (AN7 pin to AN0 pin).

Table 6-1-2 List of A/D Conversion Control Registers

Control Register	A/D Conversion Control Register (ANCTR), x'00FDA0'	
Data Buffers	A/D0 Conversion Data Buffer (AN0BUF), x'00FDA8'	A/D4 Conversion Data Buffer (AN4BUF), x'00FDAC8'
	A/D1 Conversion Data Buffer (AN1BUF), x'00FDA9'	A/D5 Conversion Data Buffer (AN5BUF), x'00FDAD'
	A/D2 Conversion Data Buffer (AN2BUF), x'00FDAA'	A/D6 Conversion Data Buffer (AN6BUF), x'00FDAE'
	A/D3 Conversion Data Buffer (AN3BUF), x'00FDAB'	A/D7 Conversion Data Buffer (AN7BUF), x'00FDAF'

The A/D conversion control register (ANCTR) sets the A/D conversion operating conditions.

The A/D conversion results for channel 7 to channel 0 are input to the A/D conversion data buffers (ANnBUF).

6-2 Analog Interface Setup Examples

6-2-1 One Channel A/D Conversion Using AN2 Pin

This section describes the one channel A/D conversion setup by software. The AN2 pin inputs the analog voltage (0 V to 5 V) and obtains the A/D conversion result.

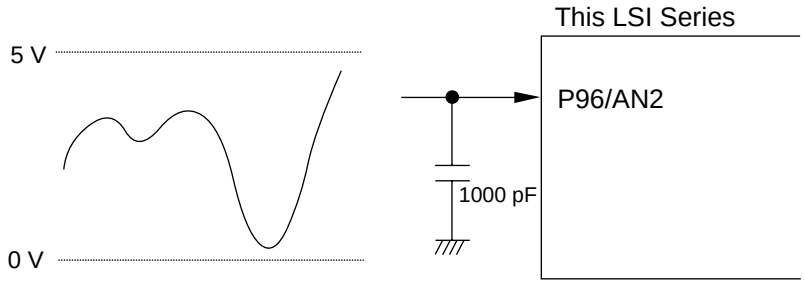


Figure 6-2-1 One Channel A/D Conversion

■ Pin Setup

(1) Set AN2 pin (P96) of the port 9 to input (P9DIR6 = '0').

■ A/D Conversion Control Register Setup

(2) Set the operating conditions to the A/D conversion control register (ANCTR). Set ANMD to 1ch/single conversion and select the clock source to SYSCLK/4 (10 MHz/4 with a 20-MHz oscillator). Set ANEN to '0' and AN1CH[2:0] to the channel number to be converted.

ANNCH[2:0] are ignored.

ANCTR: x'00FDA0'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	ANNCH2	ANNCH1	ANNCH0	-	AN1CH2	AN1CH1	AN1CH0	ANEN	ANTM1	-	-	ANCK1	ANCK0	ANMD1	ANMD0
-	0	0	0	-	0	1	0	0	0	-	-	1	0	0	0

(3) Set the ANEN flag to '1' to start the conversion. Conversion starts on the falling edge of the A/D conversion clock source after ANEN is set to 1. The conversion time is 12 cycles of the A/D conversion clock source (4.8 µs, 4.8 µs to 5.2 µs after ANEN is set).

Set the ANEN flag to 1 when starting the conversion by software.

(4) Wait for the conversion to end. Set the ANEN flag to 1 during the conversion and 0 after the conversion ends. The program waits until the ANEN flag is cleared to 0.

The CPU can read the conversion result by generating an interrupt. In this case, the CPU does not need to wait until the ANEN flag is set because an interrupt occurs after the conversion result is stored in AN2BUF.

(5) Read the A/D 2 conversion data buffer (AN2BUF). The converter divides 0 V to 5 V into 256 and the conversion result is the value from 0 to 255.

AN2BUF: x'00FDAA'

7	6	5	4	3	2	1	0
AN2 BUF7	AN2 BUF6	AN2 BUF5	AN2 BUF4	AN2 BUF3	AN2 BUF2	AN2 BUF1	AN2 BUF0

6-2-2 Multiple Channels A/D Conversion Using AN2 to AN0 pins

The AN2, AN1 and AN0 pins input the analog voltage of 0 V to 5 V and obtains the A/D conversion results. The converter performs periodically using timer 1.

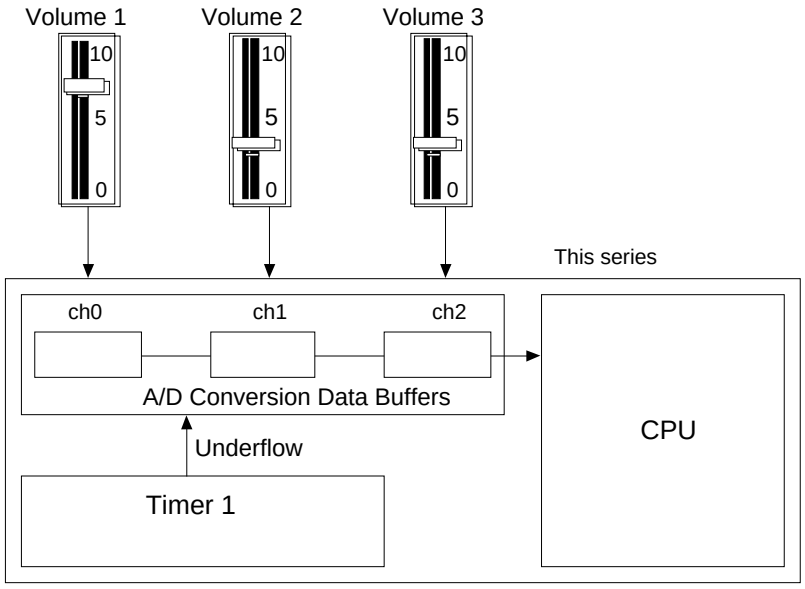


Figure 6-2-2 Multiple Channel A/D Conversion

■ A/D Conversion Control Register Setup

(1) Set the operating conditions to the A/D conversion control register (ANCTR). Set ANMD to multiple channel/single conversion and select the ANCK[1:0] bits to SYSCLK/4 (10 MHz/4 with a 20-MHz oscillator). Set ANEN and ANTM1 to '0' and '1' respectively. Set AN1CH[2:0] to the first channel number to be converted (channel 0) and ANNCH[2:0] to the last channel number to be converted (channel 2).

ANCTR: x'00FDA0'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	AN NCH2	AN NCH1	AN NCH0	-	AN 1CH2	AN 1CH1	AN 1CH0	AN EN	AN TM1	-	-	AN CK1	AN CK0	AN MD1	AN MD0
-	0	0	0	-	0	1	0	0	0	-	-	1	0	0	0

■ Timer 1 Setup

(2) Set the timer 1 divisor. Since timer 1 divides SYSCLK by 256, set the timer 1 base register (TM1BR) to 255. (The valid range for TM1BR is 1 to 255.)

TM1BR: x'00FE11'

7	6	5	4	3	2	1	0
TM1 BR7	TM1 BR6	TM1 BR5	TM1 BR4	TM1 BR3	TM1 BR2	TM1 BR1	TM1 BR0
1	1	1	1	1	1	1	1

(3) Load the TM1BR value to TM1BC. To do this, set TM1LD and TM1EN to 1 and 0 resepctively. At the same time, select the clock source.

Do not change the clock source after this step. Changing the clock source while controlling count operation will corrupt the binary counter value.

TM1MD: x'00FE21'

7	6	5	4	3	2	1	0
TM1 EN	TM1 LD	-	-	-	-	TM1 S1	TM1 S0
0	1	-	-	-	-	1	0

(4) Set both TM1LD and TM1EN of the TM1MD register to 0.

If this setting is omitted, the timer 1 binary counter may not start at the first cycle.

(5) Set TM1LD and TM1EN to 0 and 1 respectively. This starts timer 1. Counting starts at the beginning of the next cycle.

The periodical conversion saves the power consumption compared to the continuous conversion.

When the timer 1 binary counter (TM1BC) reaches 0 and loads the value of 255 from the timer 1 base register (TM1BR), a timer 1 underflow interrupt request occurs. The A/D converter converts each AN2, AN1, and AN0 once when timer 1 underflows.

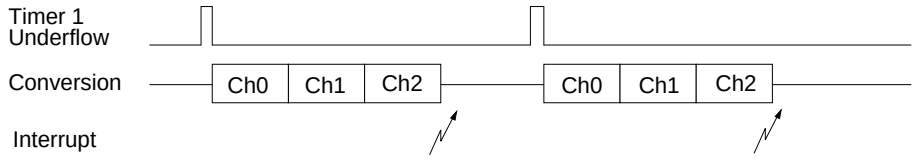


Figure 6-2-3 A/D Conversion Timing
(Single Conversion of Channel 2 to Channel 0)

Chapter 7 ATC

7

7-1 ATC

7-1-1 Overview

This series contains an Auto Transfer Control (ATC) which activates by an interrupt request. This series can transfer the data of serial interface 0 and internal RAM speedily without using the CPU.

Table 7-1-1 ATC Functions

Start	A serial 0 transmission end interrupt or serial 0 reception end interrupt
Transfer Direction	Internal RAM Æ Serial 0 Transmit/Receive Buffer (SC0TRB) Æ Internal RAM
Transfer Mode	The address for Internal RAM is x'008000' to x'0083FF' (1 KB) * One-word Transfer
Transfer End	Internal RAM Address Setting
Transfer Unit	Byte
Transfer Speed	600 ns / byte (with a 20 MHz Oscillator)
Transfer Addressing	Increment

The following is four serial interface 0 modes that the ATC can operate.

1. Synchronous Transmission Internal Clock Master (when this LSI series generates the synchronous clock)
2. Synchronous Reception External Clock Master (when this LSI series receives the synchronous clock externally)
3. Asynchronous Transmission
4. Asynchronous Reception

* Setting bi-direction of transmission and reception does not allow.

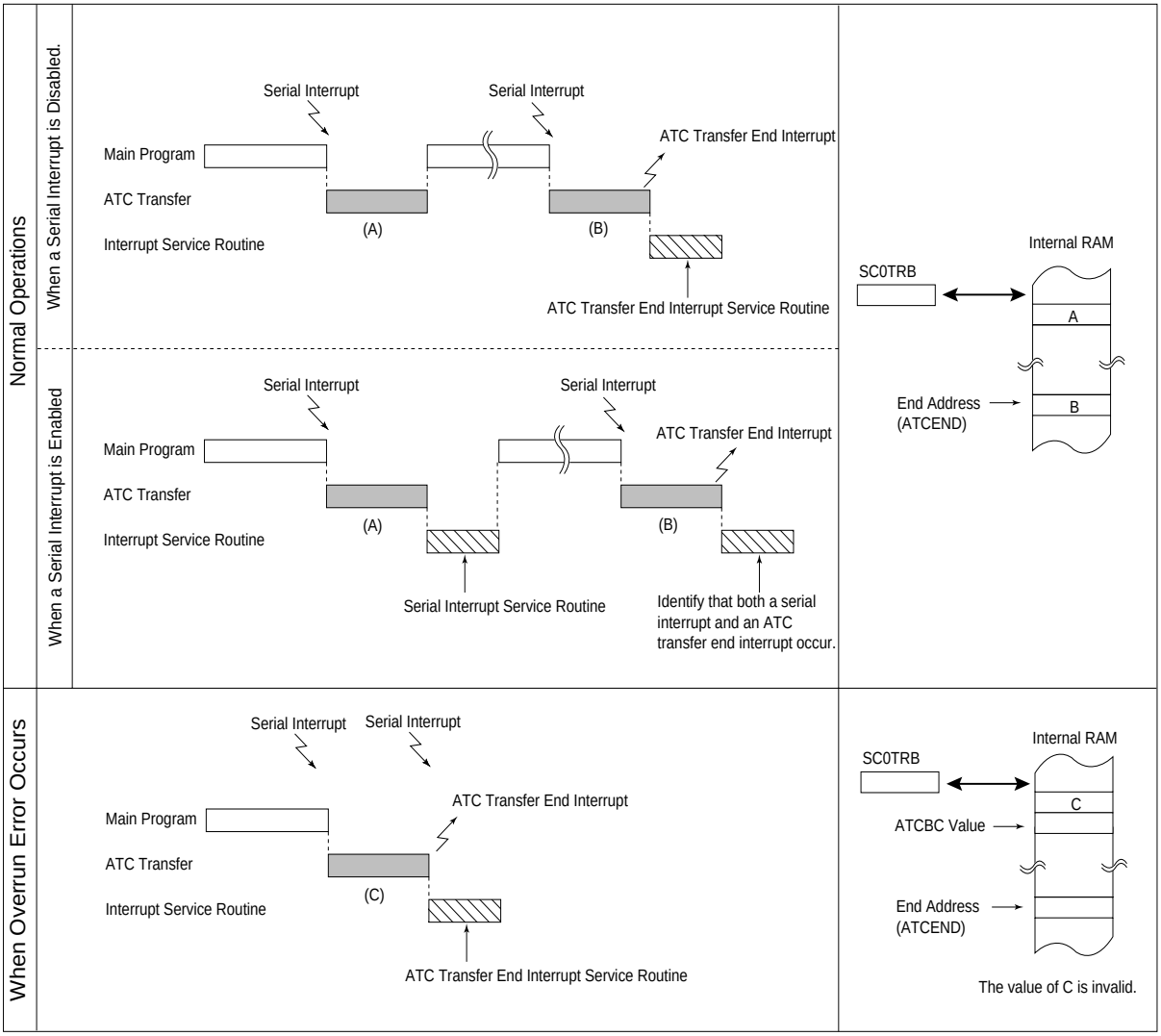


Figure 7-1-1 ATC Operations

7-1-2 Control Registers

The ATC contains the ATC control register (ATCCTR) and the ATC binary counter (ATCBC).

Table 7-1-2 List of ATC Control Registers

Control Register	ATC Control Register (ATCCTR), x'00FD10'
Counter	ATC Binary Counter (ATCBC), x'00FD12'

Set the value of the internal RAM address for ATC end greater than the value of the ATCBC counter.

The ATC control register (ATCCTR) sets the transfer direction, the internal RAM address for the ATC end and ATC enable. In addition, the ATC monitors the overrun error (*) generation.

Overrun Error *
An overrun error occurs when a next serial 0 reception end interrupt occurs before the ATC operation is completed after the serial 0 reception end interrupt occurred during the serial 0 reception (ATCDIR = ‘0’). When this error occurs, setting bit 14 (OVREF) of the ATCCTR register to 1 as well as negating bit 15 (ATCEN) ends the ATC operation forcibly. At this point, the data stored in the address which subtracted by 1 from the internal RAM address the ATCBC counter shows is invalid. (No data is stored in the address the ATCBC counter shows.)

First, the ATC binary counter (ATCBC) sets the start address of internal RAM. Next the ATCBC counter shows the RAM address to write (or read) during ATC operation.

The internal RAM area where the ATC can transfer the data is 1 k byte of x’008000’ to x’0083FF’. The upper 14 bits are fixed at ‘00000000111000’. Therefore, the lower 10 bits are read when the ATCBC counter is read. The address in the ATCCTR register or the ATCBC counter is set to only lower 10 bits.

7-2 ATC Setup Examples

7-2-1 Serial Reception

The ATC transfers the serial transmit/receive buffer contents to internal RAM automatically after the serial reception is completed. The ATC generates an ATC transfer end interrupt after the ATC transfers 5 times, and starts software processing. The start address of the ATC destination is x'00E0A0'.

■ Serial Interface 0 Setup

(1) Enable an ATC transfer end interrupt.

G6ICR: x'00FC40'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G6 LV2	G6 LV1	G6 LV0	ATC IE	TM6B IE	TM6A IE	TM6U IE	ATC IR	TM6B IR	TM6A IR	TM6U IR	ATC ID	TM6B ID	TM6A ID	TM6U ID
-	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

When a serial reception end interrupt is enabled, a serial reception end interrupt occurs each time the 1-word transfer ends.

■ ATC Setup

(2) Set the lower 10 bits of the internal RAM start address for ATC destination to the ATC binary counter (ATCBC).

ATCBC: x'00FD12'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	ATCBC 9	ATCBC 8	ATCBC 7	ATCBC 6	ATCBC 8	ATCBC 4	ATCBC 3	ATCBC 2	ATCBC 1	ATCBC 0
						0	0	1	0	1	0	0	0	0	0

(3) Set the internal RAM end address (x'00E0A4') and the transfer direction (serial → internal RAM) and clear the overrun error flag.

ATCCTR: x'00FD10'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATC EN	OVR EF	-	ATC DIR	-	-	ATCBC 9	ATCBC 8	ATCBC 7	ATCBC 6	ATCBC 8	ATCBC 4	ATCBC 3	ATCBC 2	ATCBC 1	ATCBC 0
0	0		0			0	0	1	0	1	0	0	1	0	0

(4) Set ATCEN to enable. Keep the same setting as step (3).

ATCCTR: x'00FD10'

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATC EN	OVR EF	-	ATC DIR	-	-	ATC END9	ATC END8	ATC END7	ATC END6	ATC END5	ATC END4	ATC END3	ATC END2	ATC END1	ATC END0
1	0		0			0	0	1	0	1	0	0	1	0	0

(5) Set the mode of serial interface 0. See '5-2 Serial Interface Setup Examples' for detail.

With the above setting, when the serial reception is completed, the ATC transfer the received data to memory automatically. When the ATC transfers repeatedly until the set number of operation is reached, an ATC transfer end interrupt occurs and the ATC transfer end interrupt service routine is executed.

A, B, C, D and E means 1-byte data.

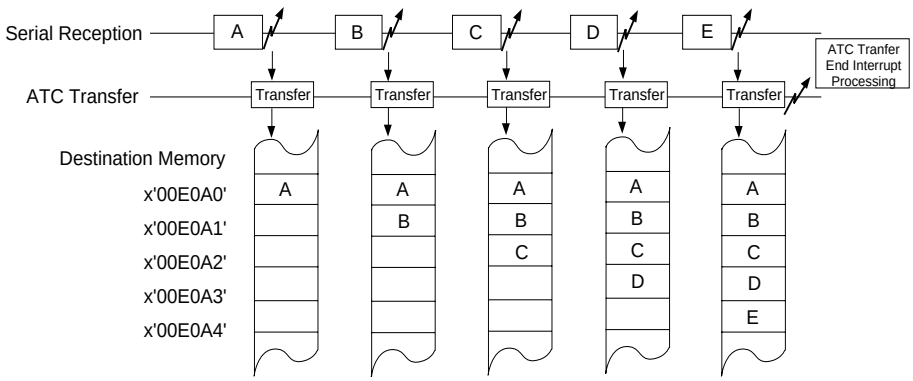


Figure 7-2-1 Serial Reception Data Transfer

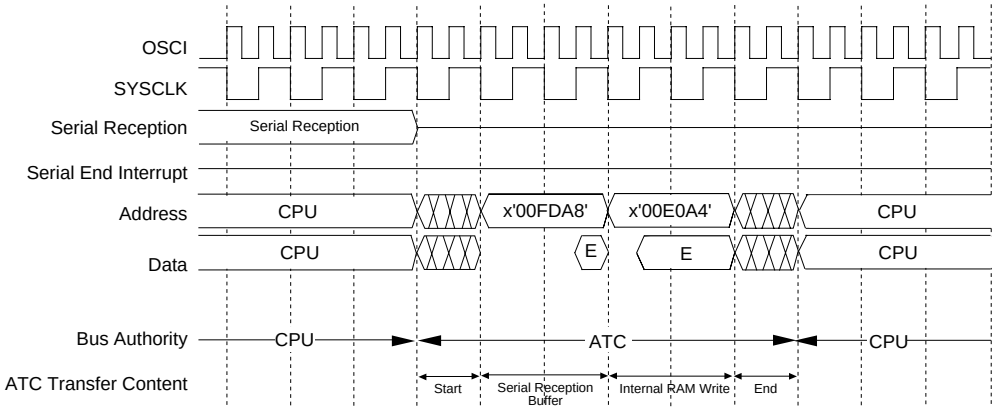


Figure 7-2-2 Last Data Transfer Timing

Chapter 8 Ports

8

8-1 Ports

8-1-1 Overview

This LSI series contains ten I/O ports. Of ports 0 to 5, port 8 and port 9 are 8 bits. Port 7 and port A are 6 bits. Port 6 is 4 bits. All ports are bidirectional. Port 0 and Port 1 control the I/O direction in 8-bit unit. Port 2 controls the I/O direction in 4-bit unit while ports 3 to A control the I/O direction in bit unit.

Table 8-1-1 Port Functions (1 of 8)

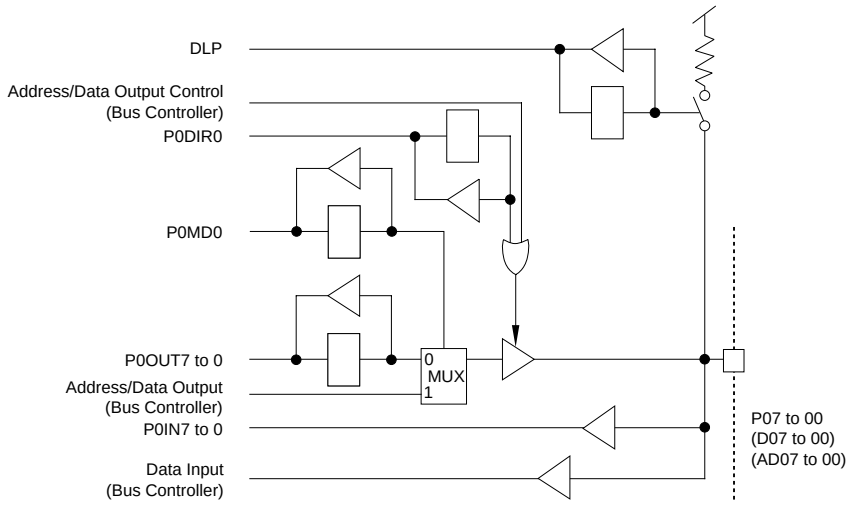
Port	Pin (Shared Pin)	Function
Port 0	P07 to P00 (D07 to D00) (AD07 to AD00)	Port 0 is used as the port 0 general-purpose port, data (address/data separated) input/output, or address/data (address/data shared) input/output. At reset, this port operates as a general-purpose port input during other modes except processor mode and as D07 to D00 (AD07 to AD00) pins during processor mode. However, this port operates as a general-purpose port during processor mode when 8-bit bus width is selected for all spaces in address/data separated mode. The mode for port 0 is selected in 8-bit unit. During processor mode (without 8-bit bus width setting for all spaces), P0MD is invalid. During memory expansion mode, set P0MD and P0DIR to 1 and 0 respectively. 

Table 8-1-1 Port Functions (2 of 8)

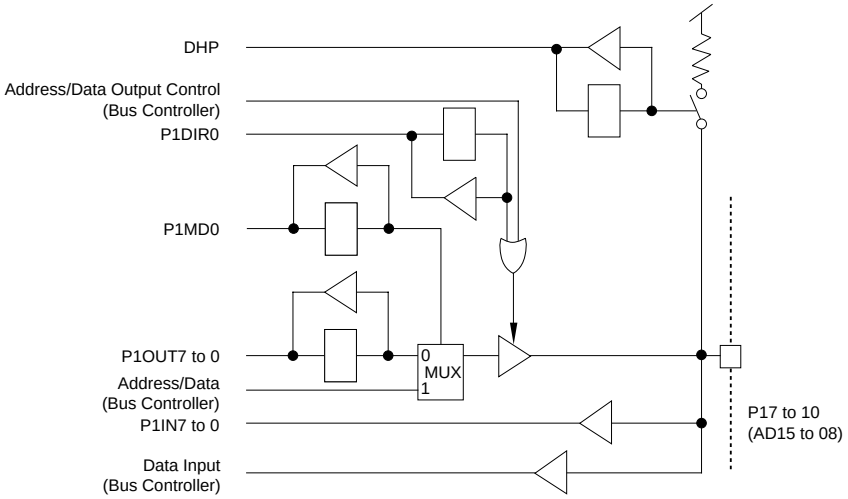
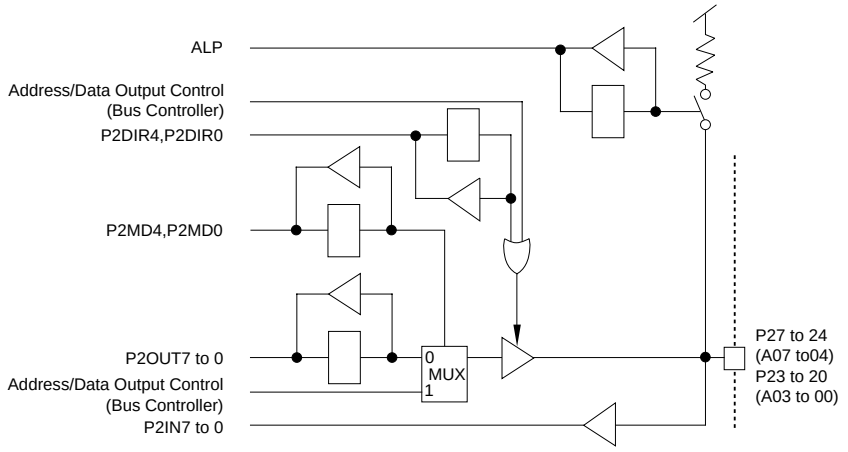
Port	Pin (Shared Pin)	Function
Port 1	P17 to P10 (D15 to D08) (AD15 to AD08)	Port 1 is used as the port 1 general-purpose port, data (address/data separated) input/output, or address/data (address/data shared) input/output. At reset, this port operates as a general-purpose port input during other modes except processor mode and as D15 to D08 (AD15 to AD08) pins during processor mode. The mode for port 1 (either port, data or address/data mode) is selected in 8-bit unit. During processor mode (without 8-bit bus width setting for all spaces), P1MD is invalid. During memory expansion mode, set P1MD and P1DIR to 1 and 0 respectively. 
Port 2	P27 to P20 (A07 to A00)	Port 2 is used as the port 2 general-purpose port or address output. At reset, this port operates as a general-purpose port input during other modes except processor mode and as A07 to A00 pins during processor mode. During processor mode, P2MD is invalid. See '2-2-1 Memory Expansion Mode (Address/Data Separated Mode)' and '2-2-3 Memory Expansion Mode (Address/Data Shared Mode)' for port setting during memory expansion mode. 

Table 8-1-1 Port Functions (3 of 8)

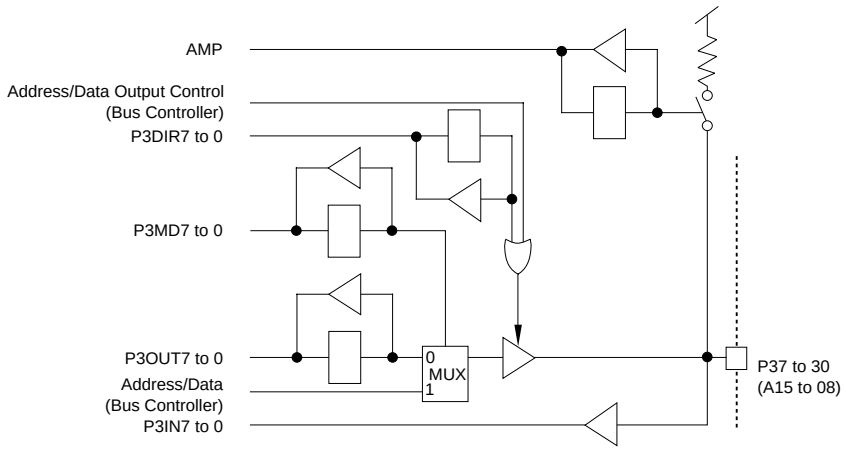
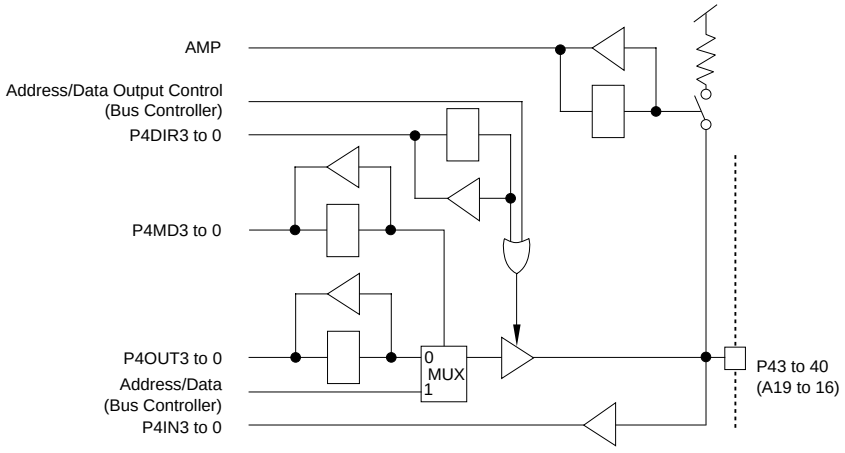
Port	Pin (Shared Pin)	Function
Port 3	P37 to P30 (A15 to A08)	Port 3 is used as the port 3 general-purpose port or address output. At reset, this port operates as a general-purpose port input during other modes except processor mode and as A15 to A08 pins during processor mode. During processor mode, P3MD is invalid. See '2-2-1 Memory Expansion Mode (Address/Data Separated Mode)' and '2-2-3 Memory Expansion Mode (Address/Data Shared Mode)' for port setting during memory expansion mode. 
Port 4	P43 to P40 (A19 to A16) P45 to P44 (A21 to A20, AN5 to AN4) P46 (A22, AN6, STOP) P47 (A23, AN7, WDOUT)	Port 4 is used as the port 4 general-purpose port, address output, A/D converter input pin or CPU status signal pin. At reset, this port operates as a general-purpose port input during other modes except processor mode and as A21 to A16 pins (P47 and P46 operate as general-purpose input) during processor mode. During processor mode, P4MD of P45 to P40 is invalid. See '2-2-1 Memory Expansion Mode (Address/Data Separated Mode)' and '2-2-3 Memory Expansion Mode (Address/Data Shared Mode)' for port setting during memory expansion mode. 

Table 8-1-1 Port Functions (4 of 8)

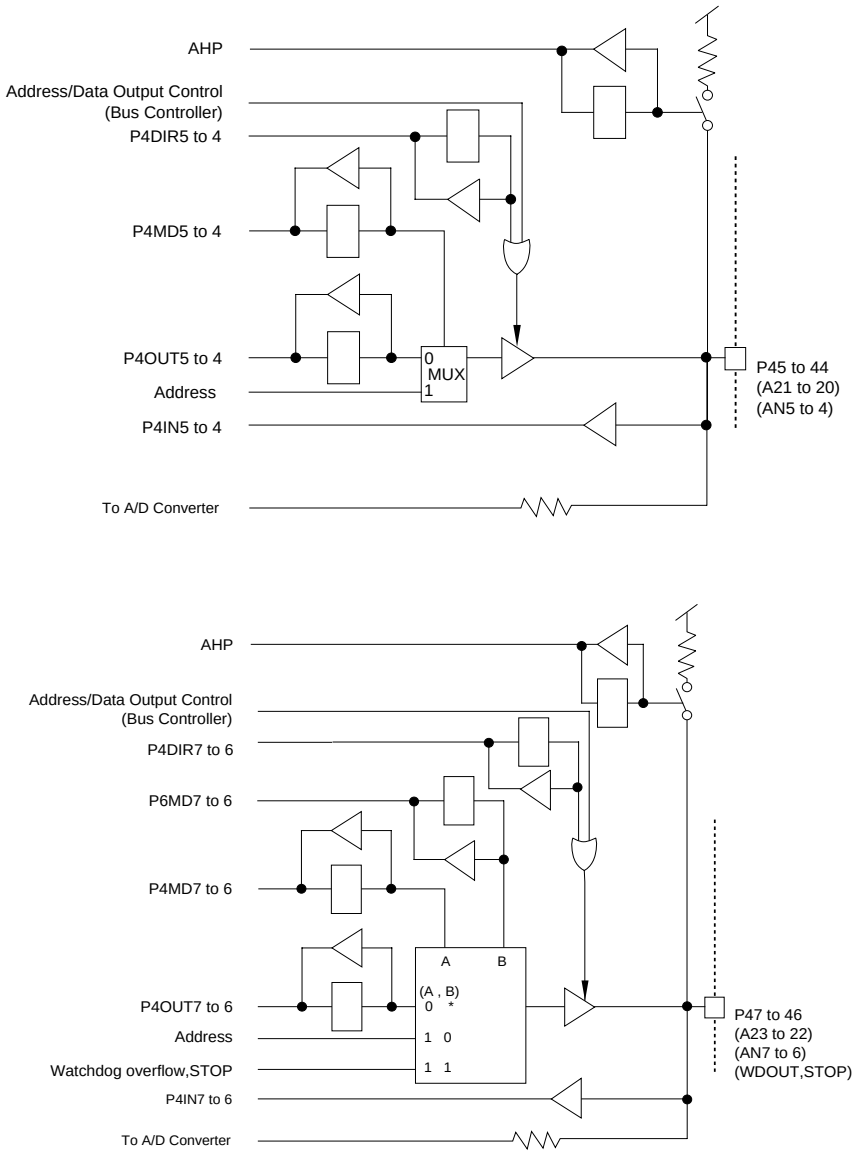
Port	Pin (Shared Pin)	Function
Port 4		

Table 8-1-1 Port Functions (5 of 8)

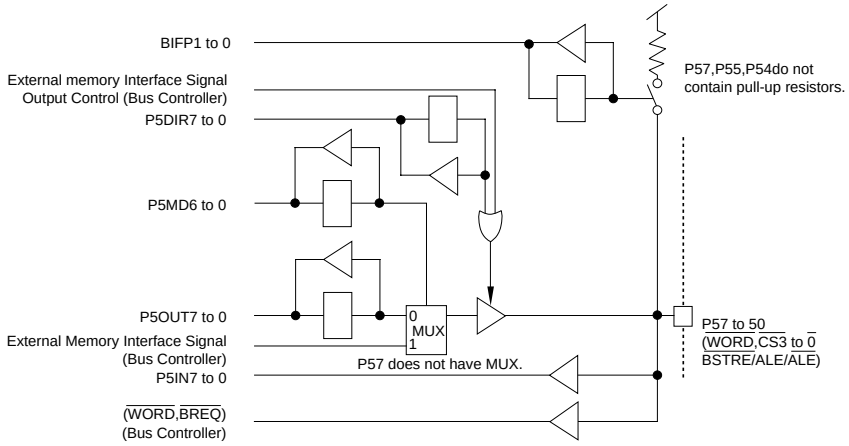
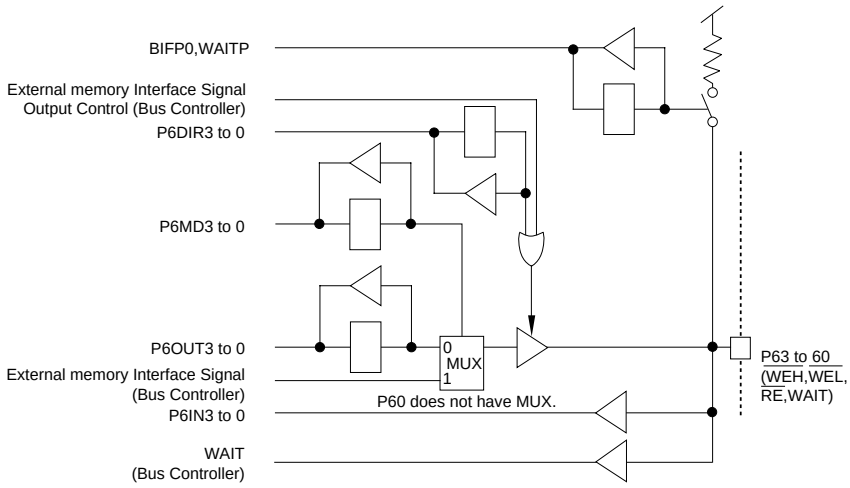
Port	Pin (Shared Pin)	Function
Port 5	P57 to P50 ($\overline{\text{WORD}}$, $\overline{\text{BSTRE}}$, ALE, $\overline{\text{ALE}}$, $\overline{\text{BRACK}}$, $\overline{\text{BREQ}}$, $\overline{\text{CS3}}$ to $\overline{\text{CS0}}$)	Port 5 is used as the port 5 general-purpose port or external memory interface signals pins ($\overline{\text{WORD}}$, $\overline{\text{BSTRE}}$, ALE, $\overline{\text{ALE}}$, $\overline{\text{BRACK}}$, $\overline{\text{BREQ}}$, $\overline{\text{CS3}}$ to $\overline{\text{CS0}}$). At reset, this port operates as a general-purpose port input during other modes except processor mode while P56, P53 to P50 pins operate as $\overline{\text{BSTRE}}$, ALE, $\overline{\text{ALE}}$, $\overline{\text{BRACK}}$, $\overline{\text{BREQ}}$, $\overline{\text{CS3}}$ to $\overline{\text{CS0}}$ pins during processor mode. During processor mode, P5MD6, P5MD3 to P5MD0 are invalid. 
Port 6	P63 to P60 ($\overline{\text{WEL}}$, $\overline{\text{WEH}}$, $\overline{\text{RE}}$, WAIT)	Port 6 is used as the port 6 general-purpose port or external memory interface signals pins (WAIT, $\overline{\text{RE}}$, $\overline{\text{WEH}}$, $\overline{\text{WEL}}$). At reset, this port operates as a general-purpose port input during other modes except processor mode while P63 to P61 pins operate as $\overline{\text{WEH}}$, $\overline{\text{WEL}}$ and $\overline{\text{RE}}$ pins during processor mode. During processor mode, P6MD3 to P6MD1 are invalid. 

Table 8-1-1 Port Functions (6 of 8)

Port	Pin (Shared Pin)	Function
Port 7	P75 (SBO1) P74 (SBI1) P73 (SBT1) P72 (SBO0) P71 (SBI0) P70 (SBT0)	Port 7 is used as the port 7 general-purpose port or serial interface signal pins. At reset, this port operates as a general-purpose port input.

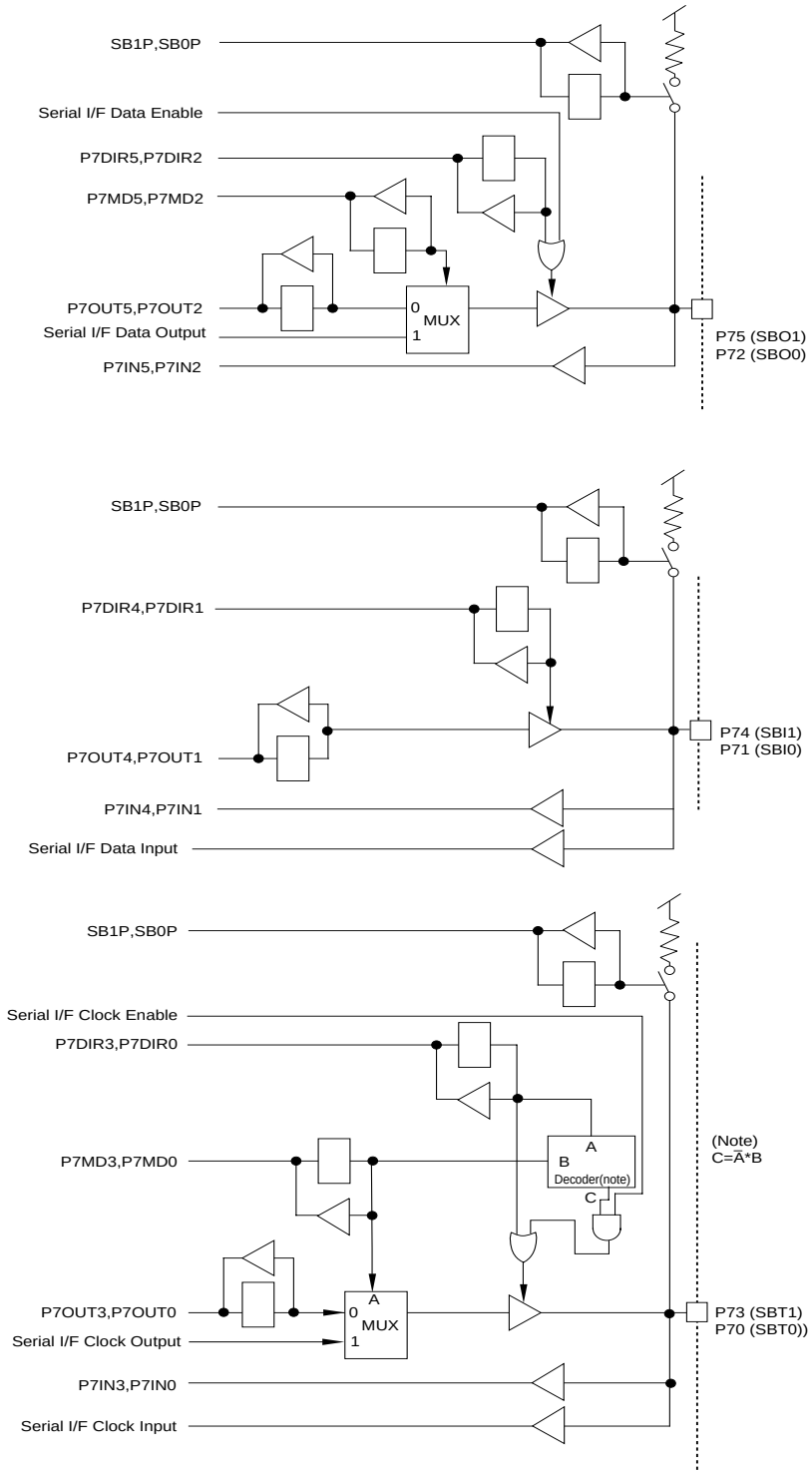


Table 8-1-1 Port Functions (7 of 8)

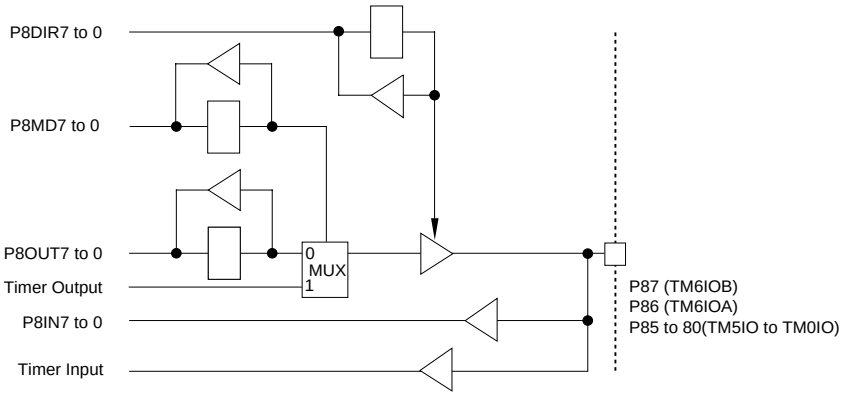
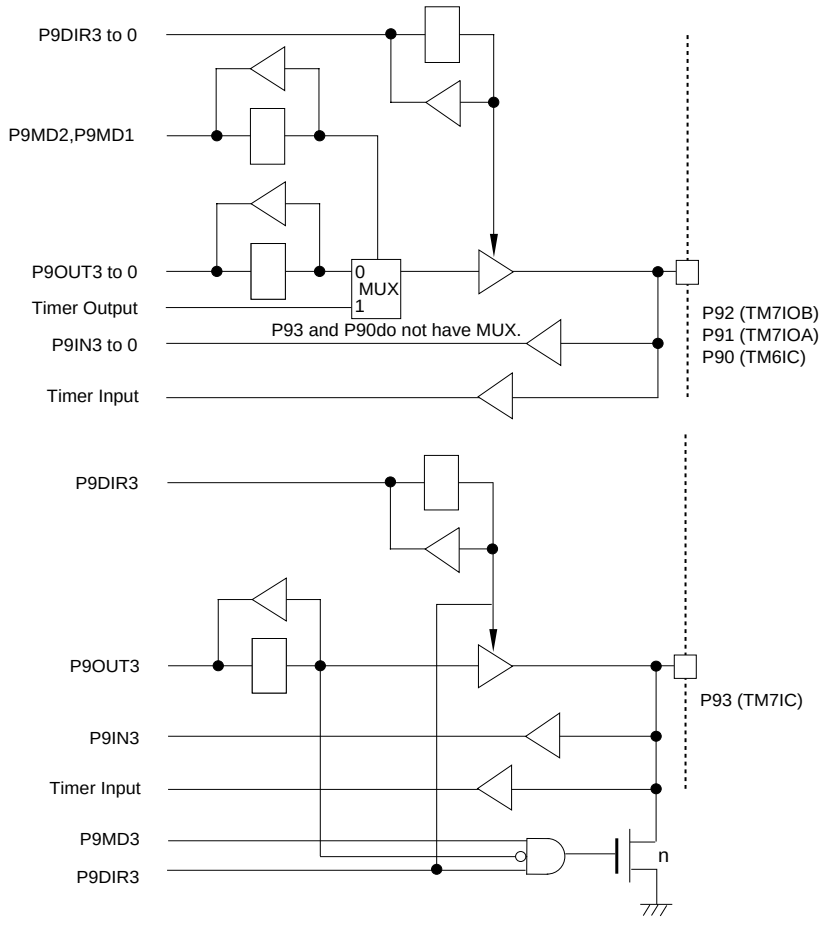
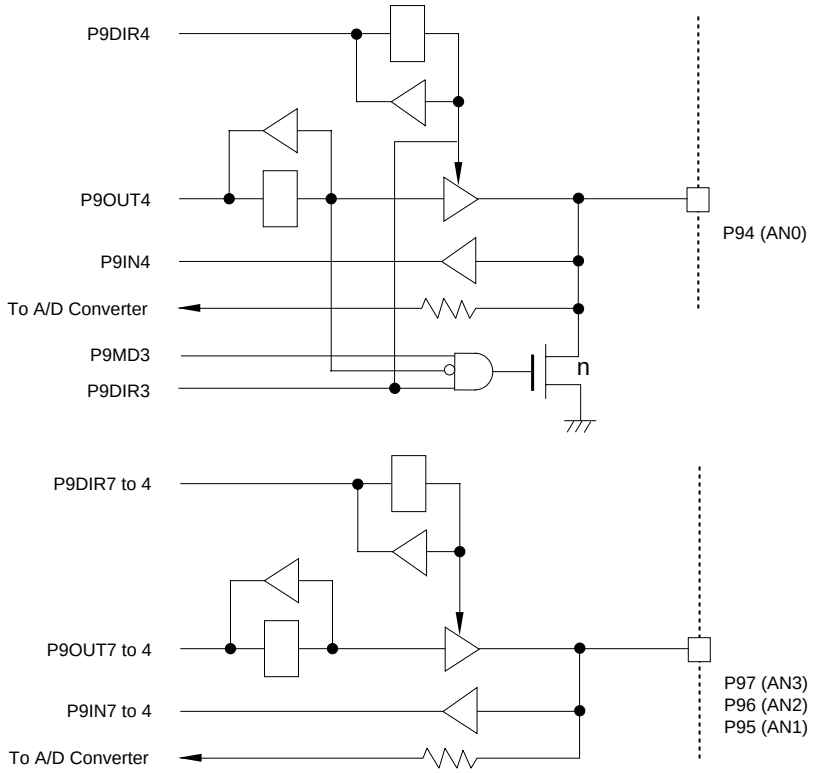
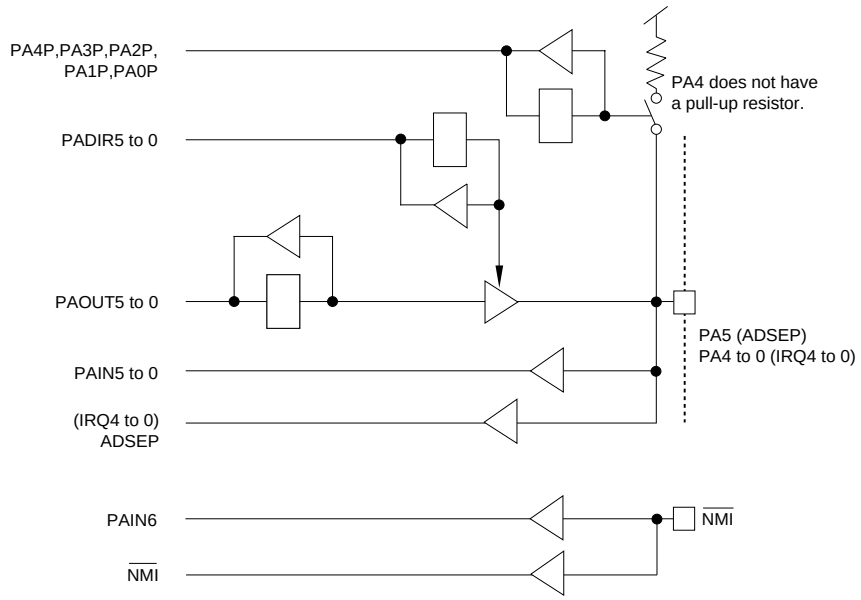
Port	Pin (Shared Pin)	Function
Port 8	P87 (TM6IOB) P86 (TM6IOA) P85 to P80 (TM5IO to TM0IO)	Port 8 is used as the port 8 general-purpose port or timer input/output pins (TM0IO to TM5IO, TM6IOA, TM6IOB). At reset, this port operates as a general-purpose port input. 
Port 9	P97 to P94 (AN3 to AN0) P93 (TM7IC) P92 (TM7IOB) P91 (TM7IOA) P90 (TM6IC)	Port 9 is used as the port 9 general-purpose port, timer input/output pins or A/D converter input pins (AN3 to AN0, TM7IC, TM7IOB, TM7IOA, TM6IC). At reset, this port operates as a general-purpose port input. 

Table 8-1-1 Port Functions (8 of 8)

Port	Pin (Shared Pin)	Function
Port 9		
Port A	PA5 (ADSEP) PA4 to PA0 (IRQ4 to IRQ0)	Port A is used as the port A general-purpose port or interrupt related signal pins (ADSEP, IRQ4 to IRQ0). At reset, this port operates as a general-purpose port input. This port can read the level of $\overline{\text{NMI}}$ pin by operating as the port input pin (PAIN6), and verify an error due to chattering using software. 

8-1-2 Control Registers

This section describes the port control registers.

Table 8-1-2 List of Port Control Registers

Port 0	Port 0 Output Register Port 0 Input Register Port 0 Input/Output Control Register Port 0 Output Mode Register	P0OUT P0IN P0DIR P0MD	x'00FFC0' x'00FFD0' x'00FFE0' x'00FFF0'
Port 1	Port 1 Output Register Port 1 Input Register Port 1 Input/Output Control Register Port 1 Output Mode Register	P1OUT P1IN P1DIR P1MD	x'00FFC1' x'00FFD1' x'00FFE1' x'00FFF1'
Port 2	Port 2 Output Register Port 2 Input Register Port 2 Input/Output Control Register Port 2 Output Mode Register	P2OUT P2IN P2DIR P2MD	x'00FFC2' x'00FFD2' x'00FFE2' x'00FFF2'
Port 3	Port 3 Output Register Port 3 Input Register Port 3 Input/Output Control Register Port 3 Output Mode Register	P3OUT P3IN P3DIR P3MD	x'00FFC3' x'00FFD3' x'00FFE3' x'00FFF3'
Port 4	Port 4 Output Register Port 4 Input Register Port 4 Input/Output Control Register Port 4 Output Mode Register	P4OUT P4IN P4DIR P4MD	x'00FFC4' x'00FFD4' x'00FFE4' x'00FFF4'
Port 5	Port 5 Output Register Port 5 Input Register Port 5 Input/Output Control Register Port 5 Output Mode Register	P5OUT P5IN P5DIR P5MD	x'00FFC5' x'00FFD5' x'00FFE5' x'00FFF5'
Port 6	Port 6 Output Register Port 6 Input Register Port 6 Input/Output Control Register Port 6 Output Mode Register	P6OUT P6IN P6DIR P6MD	x'00FFC6' x'00FFD6' x'00FFE6' x'00FFF6'
Port 7	Port 7 Output Register Port 7 Input Register Port 7 Input/Output Control Register Port 7 Output Mode Register	P7OUT P7IN P7DIR P7MD	x'00FFC7' x'00FFD7' x'00FFE7' x'00FFF7'

Port 8	Port 8 Output Register Port 8 Input Register Port 8 Input/Output Control Register Port 8 Output Mode Register	P8OUT P8IN P8DIR P8MD	x'00FFC8' x'00FFD8' x'00FFE8' x'00FFF8'
Port 9	Port 9 Output Register Port 9 Input Register Port 9 Input/Output Control Register Port 9 Output Mode Register	P9OUT P9IN P9DIR P9MD	x'00FFC9' x'00FFD9' x'00FFE9' x'00FFF9'
Port A	Port A Output Register Port A Input Register Port A Input/Output Control Register	PAOUT PAIN PADIR	x'00FFCA' x'00FFDA' x'00FFEA'
Other	Port Pull-up Control Register Word Data Byte Swap Register Pointer Data Byte Swap Register L Pointer Data Byte Swap Register H Long-word data Byte Swap Register L Long-word data Byte Swap Register H	PPLU WBSWP PBSWPL PBSWPH LBSWPL LBSWPH	x'00FFB0' x'00FFA0' x'00FFA2' x'00FFA4' x'00FFA6' x'00FFA8'

The port output register (PnOUT) sets the data to be output. The port input register (PnIN) reads the pin values. The port input/output control register (PnDIR) sets the input or output of all bits or each bit. The output mode register (PnMD) selects the port output. The port pull-up control register (PPLU) selects on/off of each pin.

The pullup resistor is approximately 30 kΩ. See the product specifications for the exact value.

■ P07 to P00 Pins

Selection	P0DIR0	P0MD0	Description
Port Input	0	0	Select the port input or the port output only when 8-bit bus width for all spaces is selected during single-chip mode or address/data separated mode (the word pin is high and all 8th bits of the MEMMD3 to MEMMD1 registers are high).
Port Output	1	0	
D07 to D00/ AD07 to AD00	0	1	Select D07 to D00 during address/data separated mode, AD07 to AD00 during address/data shared mode.
Reserved	1	1	-

Note: Set only in 8-bit unit.

■ P17 to P10 Pins

Selection	P1DIR0	P1MD0	Description
Port Input	0	0	Select the port input or the port output only when single-chip mode is selected.
Port Output	1	0	
D15 to D08/ AD15 to AD08	0	1	Select D15 to D08 during address/data separated mode, AD15 to AD08 during address/data shared mode.
Reserved	1	1	-

Note: Set only in 8-bit unit.

■ P23 to P20 Pins

Selection	P2DIR0	P2MD0	Description
Port Input	0	0	Do not select the port input or the port output in address/data separated mode during processor mode.
Port Output	1	0	
A03 to A00	0	1	-
Reserved	1	1	-

Note: Set only in 4-bit unit.

■ P27 to P24 Pins

Selection	P2DIR4	P2MD4	Description
Port Input	0	0	Do not select the port input or the port output in address/data separated mode during processor mode.
Port Output	1	0	
A07 to A04	0	1	-
Reserved	1	1	-

Note: Set only in 4-bit unit.

■ P37 to P30 Pins

Selection	P3DIRn (n=7 to 0)	P3MDn (n=7 to 0)	Description
Port Input	0	0	Do not select the port input or the port output in address/data separated mode during processor mode.
Port Output	1	0	
A15 to A08	0	1	-
Reserved	1	1	-

■ P43 to P40 Pins

Selection	P4DIRn (n=3 to 0)	P4MDn (n=3 to 0)	Description
Port Input	0	0	Do not select the port input or the port output during processor mode.
Port Output	1	0	
A19 to A16	0	1	-
Reserved	1	1	-

■ P45 to P44 Pins

Selection	P4DIRn (n=5, 4)	P4MDn (n=5, 4)	Description
Port Input	0	0	Do not select the port input or the port output during processor mode.
AN5, 4 Input			
Port Output	1	0	
A21, A20	0	1	-
Reserved	1	1	-

■ P46 Pin

Selection	P4DIR6	P4MD6	P6MD6
Port Input	0	0	*
AN6 Input			
Port Output	1	0	*
A22 Output	0	1	0
STOP Output	1	1	1
Reserved	1	1	0

■ P47 Pin

Selection	P4DIR7	P4MD7	P6MD7
Port Input	0	0	*
AN7 Input			
Port Output	1	0	*
A23 Output	0	1	0
WDOUT Output	0	1	1
Reserved	1	1	0

■ P53 to P50 Pins

Selection	P5DIRn (n=3 to 0)	P5MDn (n=3 to 0)	Description
Port Input	0	0	Do not select the port input or the port output during processor mode.
Port Output	1	0	
/CS Output	0	1	-
Reserved	1	1	-

■ P54 Pin

Selection	P5DIR4	P5MD4
Port Input	0	0
Port Output	1	0
/BREQ Output	0	1
Reserved	1	1

■ P55 Pin

Selection	P5DIR5	P5MD5
Port Input	0	0
Port Output	1	0
/BREQ Output	1	1
Reserved	0	1

■ P56 Pin

Selection	P5DIR6	P5MD6	Description
Port Input	0	0	Do not select the port input or the port output during processor mode.
Port Output	1	0	
$\overline{\text{BSTRE}}$, ALE, $\overline{\text{ALE}}$	0	1	Select $\overline{\text{BSTRE}}$ during address/data separated mode, ALE ($\overline{\text{ALE}}$) during address/data shared mode.
Reserved	1	1	-

■ P57 Pin

Selection	P5DIR7	Description
Port Input	0	Select the port input during single-chip mode. Otherwise, select $\overline{\text{WORD}}$ input.
$\overline{\text{WORD}}$ Input		
Port Output	1	

■ P60 Pin

Selection	P6DIR0	Description
Port Input WAIT Input	0	Select WAIT input when the clock is set to handshake mode. Otherwise, select the port input.
Port Output	1	-

■ P63 to P61 Pins

Selection	P6DIRn (n=3 to 1)	P6MDn (n=3 to 1)	Description
Port Input	0	0	Do not select the port input or the port output during processor mode.
Port Output	1	0	
$\overline{WEH}$, $\overline{WEL}$. $\overline{RE}$ Output	0	1	-
Reserved	1	1	-

■ P73 and P70 Pins

Selection	P7DIRn (n=3,0)	P7MDn (n=3,0)	Description
Port Input Serial Clock Input	0	0	Operate as a serial clock input pin when setting the serial clock source to the SBT pin (including I^2C mode).
Serial Clock I/O (Half-duplex)	0	1	Become output only when this LSI series output during bidirectional synchronous transfer.
Port Output	1	0	-
Serial Clock Output	1	1	-

■ P74 and P71 Pins

Selection	P7DIRn (n=4, 1)	Description
Port Input Serial Input	0	Operate as a serial data input pin when the serial reception is enabled.
Port Output	1	-

■ P75 and P72 Pins

Selection	P7DIRn (n=5, 2)	P7MDn (n=5, 2)	Description
Port Input	0	*	Select the port input during I^2C mode.
Port Output	1	0	-
Serial Output	1	1	-

■ P87 to P80 Pins

Selection	P8DIRn (n=7 to 0)	P8MDn (n=7 to 0)	Description
Port Input Timer Input	0	*	Operate as a timer input pin when selecting the timer closk source to the pin.
Port Output	1	0	-
Timer Output	1	1	-

■ P90 Pin

Selection	P9DIR0	Description
Port Input Serial Input	0	Operate as a serial data input pin when selecting the 16-bit timer binary counter clear condition 2 (5th bit of TM6MD).
Port Output	1	-

■ P92 and P91 Pins

Selection	P9DIRn (n=2, 1)	P9MDn (n=2, 1)	Description
Port Input Timer Input	0	*	Operate as a timer input pin when setting the timer closk source, capture, trigger and encoder.
Port Output	1	0	-
Timer Output	1	1	-

■ P93 Pin

Selection	P9DIR3	P9MD3	Description
Port Input Timer Input	0	*	Operate as a serial data input pin when selecting the 16-bit timer binary counter clear condition 2 (5th bit of TM6MD).
Port Output	1	0	LED drive is enabled when P9MD3 is set to 1. P9OUT3 selects light ON or OFF.
LED Output		1	

■ P93 Pin

Selection	P9DIR4	P9MD4	Description
Port Input Timer Input	0	*	-
Port Output LED Output	1	0 1	LED drive is enabled when P9MD4 is set to 1. P9OUT4 selects light ON or OFF.

■ P97 to P95 Pins

Selection	P9DIRn (n=7 to 4)
Port Input AN3 to 0 Input	0
Port Output	1

■ PA4 to PA0 Pins

Selection	PADIRn (n=4 to 0)
Port Input Interrupt Input	0
Port Output	1

■ PA5 Pin

Selection	PADIR5	Description
Port Input ADSEP Input	0	Operate as the port input only during single-chip mode. Otherwise, operate as the ADSEP input.
Port Output	1	Operate as the port output only during single-chip mode. This operation is not guaranteed in other modes.

8-2 Byte Swap Registers

8-2-1 Overview

This LSI series contains a word byte swap register, point byte swap registers and long word swap registers. The data is swapped and read as Figure 8-2-1 shows.

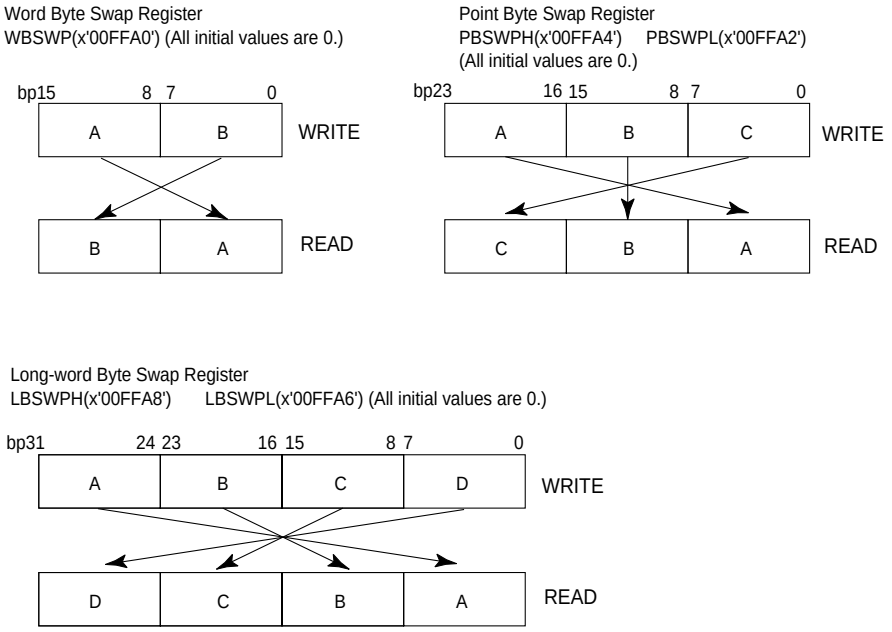


Figure 8-2-1 Byte Swap Register

8-3 Pull-up Control Register

8-3-1 Overview

This LSI series contains a pin which sets a pull-up resistor using the program. See ‘9-2-3 List of Pin Functions’.

Table 8-3-1 Pull-up Control Register

Bit	Corresponded Pin Number	Description
0	84 to 91	D07 to D00, AD07 to AD00, P07 to P00
1	93 to 100	D15 to D08, AD15 to AD08, P17 to P11
2	13 to 16, 26 to 29	A07 to A00, P27 to P20
3	30 to 33, 35 to 38	A15 to A08, P37 to P30
4	39 to 42, 44 to 47	A23 to A16, P47 to P40
5	1	WAIT, P60
6	2 to 4, 11	/RE, /WEH, /WEL, /BSTRE, P63 to P61, P56
7	5 to 8	/CS3 to /CS0, P53 to P50
8	76	/IRQ0, PA0
9	77	/IRQ1, PA1
10	78	/IRQ2, PA2
11	79	/IRQ3, PA3
12	80	/IRQ4, PA4
13	67 to 69	SBT0, SBI0, SBO0, P72 to P70
14	70 to 72	SBT1, SBI1, SBO1, P75 to P73
15	Reserved	Always set to 0.

Chapter 9 Appendix

9

9-1 Electrical Characteristics

9-1-1 Electrical Characteristics 5 V

Structure	CMOS integrated circuit
Application	General purpose
Function	16-bit microcontroller
Pin Configuration	Figure 1-4-1
External Dimensions	Figure 1-5-1

A. Absolute Maximum Ratings

VSS = 0 V

Parameter		Symbol	Rating	Unit
A1	Power supply voltage	V_{DD}	- 0.3 to + 7.0	V
A2	Input pin voltage	V_I	- 0.3 to V_{DD} + 0.3	V
A3	Output pin voltage	V_O	- 0.3 to V_{DD} + 0.3	V
A4	Input/output pin voltage	V_{IO}	- 0.3 to V_{DD} + 0.3	V
A5	Operating ambient temperature	Topr	- 40 to + 85	C
A6	Storage temperature	Tstg	-55 to + 125	C

Note:

1. Absolute Maximum Ratings are stress ratings not to cause damage to the device. Operation at these ratings is not guaranteed.
2. All of the VDD and Vss pins are external pins. Connect them directly to the power source and ground.
3. To prevent latch-up tolerance, connect more than one by-pass condenser between power supply pins and ground. Use at least 0.2 mF condenser.

B. Operating Conditions

V_{SS} = 0 V
Ta = -40 C to +85 C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
B1	Power supply voltage	V_{DD}		4.5	5	5.5	V
	Crystal Oscillator 1 (OSCI)						
B2	Oscillator frequency	Fosc1		4		22.6	MHz
	Crystal Oscillator 2 (XI)						
B3	Oscillator frequency	Fosc2		32		200	kHz

MN102L610B does not contain flash memory

B. Flash Programming Operating Conditions

V_{SS} = 0 V
Ta = 0 C to +70 C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
B4	Power supply voltage	V_{DD}	During programming	4.5	5	5.5	V
B5	Guaranteed programming time		To each block			100	time
B6	Oscillator frequency		128 KB entirely erase		1	2.5	s
B7	Write time		4 Byte write VDD=5.0 V T=25 C		50	250	μs/4Byte

C. Electrical Characteristics

1. DC Characteristics

V_{DD} = 5.0 V
V_{SS} = 0 V
Ta = -40 C to +85 C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
C1	Power supply current during operation	$I_{DD}1$	$V_I = V_{DD}$ or V_{SS} Fosc1 = 22.6 MHz Output pins open			75	mA
C2	Power supply current during slow mode	$I_{DD}2$	$V_I = V_{DD}$ or V_{SS} Fosc2 = 32 kHz Output pins open			10	mA
C3	Power supply current in STOP mode	$I_{DD}3$	Oscillator stop All functions stop			50	μA
C4	Power supply current in HALT0 mode	$I_{DD}4$	Fosc1 = 22.6 MHz Fosc2 = 32 kHz			30	mA
C5	Power supply current in HALT1 mode	$I_{DD}5$	Fosc1 = Oscillator stop Fosc2 = 32 kHz			1	mA

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C

	Parameter	Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Input/Output Pins 1 < Output pushpull/Input TTL level schmidt trigger > TMnIO(n=0 to 5), TMnIOA(n=6, 7), TMnIOB(n=6, 7), TM6IC, ADSEP							
C6	Input high voltage	V_{IH1}		2.4			V
C7	Input high voltage	V_{IL1}	Other than above			0.8	V
C8	Output high voltage	V_{OH1}	V_{DD} = 5.0 V I_{OH} = -4.0 mA	V_{DD}-0.6			V
C9	Output low voltage	V_{OL1}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C10	Output leakage current	I_{LO1}	Vo = Hi-z			±10	μA
Input/Output Pins 2 < Output pushpull/Input TTL level schmitt trigger/Programmable pullup > SBO1, SBI1, SBT1, SBO0, SBI0, SBT0							
C11	Input high voltage	V_{IH2}		2.4			V
C12	Input low voltage	V_{IL2}				0.8	V
C13	Output high voltage	V_{OH2}	V_{DD} = 5.0 V I_{OH} = -4.0 mA	V_{DD}-0.6			V
C14	Output low voltage	V_{OL2}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C15	Output leakage current	I_{LO2}	Vo = Hi-z			±10	μA
C16	Pullup resistance	P_{PU1}	V_{DD} = 5.0 V V_I = 1.5 V	10	30	50	kΩ

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C

	Parameter	Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Input/Output Pins 3 < Output pushpull/Input TTL level schmitt trigger/Programmable pullup > WAIT, /RE, /WEL, /WEH, /CS3 to /CS0, ALE, A19 to A0, /IRQ4 to /IRQ0							
C17	Input high voltage	V_{IH3}		2.4			V
C18	Input low voltage	V_{IL3}				0.8	V
C19	Output high voltage	V_{OH3}	V_{DD} = 5.0 V I_{OH} = -2.0 mA	V_{DD}-0.6			V
C20	Output low voltage	V_{OL3}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C21	Output leakage current	I_{LO3}	Vo = Hi-z			±10	μA
C22	Pullup resistance	P_{PU2}	V_{DD} = 5.0 V V_I = 1.5 V	10	30	50	kΩ
Input/Output Pins 4 < Output pushpull/Input TTL level schmitt trigger > /BREQ, /BRACK, /WORD							
C23	Input high voltage	V_{IH4}		2.4			V
C24	Input low voltage	V_{IL4}				0.8	V
C25	Output high voltage	V_{OH4}	V_{DD} = 5.0 V I_{OH} = -2.0 mA	V_{DD}-0.6			V
C26	Output low voltage	V_{OL4}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C27	Output leakage current	I_{LO4}	Vo = Hi-z			±10	μA

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C

	Parameter	Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Input/Output Pins 5 < Output pushpull/Input TTL level schmitt trigger/Programmable pullup > D15 to D0							
C28	Input high voltage	V_{IH5}		2.4			V
C29	Input low voltage	V_{IL5}				0.8	V
C30	Output high voltage	V_{OH5}	V_{DD} = 5.0 V I_{OH} = -2.0 mA	V_{DD}-0.6			V
C31	Output low voltage	V_{OL5}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C32	Output leakage current	I_{LO5}	Vo = Hi-z			±10	μA
C33	Pullup resistance	P_{PU3}	V_{DD} = 5.0 V V_I = 1.5 V	10	30	50	kΩ
Input/Output Pins 5 < Output pushpull/Analog Input > AN3 to AN1							
C34	Input high voltage	V_{IH6}		V_{DD}x0.8			V
C35	Input low voltage	V_{IL6}				V_{DD}x0.2	V
C36	Output high voltage	V_{OH6}	V_{DD} = 5.0 V I_{OH} = -4.0 mA	V_{DD}-0.6			V
C37	Output low voltage	V_{OL6}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C38	Output leakage current	I_{LO6}	Vo = Hi-z			±10	μA

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C

	Parameter	Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Input/Output Pins 7 < Output pushpull/Analog Input/Programmable pullup > A23 to A20							
C39	Input high voltage	V_{IH7}		V_{DD}x0.8			V
C40	Input low voltage	V_{IL7}				V_{DD}x0.2	V
C41	Output high voltage	V_{OH7}	V_{DD} = 5.0 V I_{OH} = -4.0 mA	V_{DD}-0.6			V
C42	Output low voltage	V_{OL7}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C43	Output leakage current	I_{LO7}	Vo = Hi-z			±10	μA
C44	Pullup resistance	P_{PU4}	V_{DD} = 5.0 V V_I = 1.5 V	10	30	50	kΩ
Input/Output Pins 8 < Input CMOS level schmitt trigger/Output open-drain/Pullup > /RST							
C45	Input high voltage	V_{IH8}		V_{DD}x0.9			V
C46	Input low voltage	V_{IL8}				V_{DD}x0.1	V
C47	Pullup resistance	P_{PU5}	V_{DD} = 5.0 V V_I = 1.5 V	10	30	50	kΩ

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
I/O Pin 9 < Output pushpull / Input TTL level shumitt > TM7IC							
C48	Input high voltage	V_{IH9}		2.4			V
C49	Input low voltage	V_{IL9}				0.8	V
C50	Output high voltage	V_{OH8}	V_{DD} = 5.0 V I_{OH} = -4.0 mA	V_{DD}-0.6			V
C51	Output low voltage1	V_{OL8}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C52	Output low voltage2	V_{OL9}	During LED ouput VDD = 5.0 V I_{OH} = 34.0 mA			0.8	V
C53	Output leakage current	I_{LO8}	V_O = Hi-z			±10	μA
I/O Pin 10 < Output pushpull / Analog input > AN0							
C54	Input high voltage	V_{IH10}		V_{DD}x0.8			V
C55	Input low voltage	V_{IL10}				V_{DD}x0.2	V
C56	Output high voltage	V_{OH9}	V_{DD} = 5.0 V I_{OH} = -4.0 mA	V_{DD}-0.6			V
C57	Output low voltage1	V_{OL10}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
C58	Output low voltage2	V_{OL11}	During LED ouput VDD = 5.0 V I_{OH} = 34.0 mA			0.8	V
C59	Output leakage current	I_{LO9}	V_O = Hi-z			±10	μA

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Output Pin < Output pushpull > SYSCLK							
C60	Output high voltage	V_{OH8}	V_{DD} = 5.0 V I_{OH} = -4.0 mA	V_{DD}-0.6			V
C61	Output low voltage	V_{OL8}	V_{DD} = 5.0 V I_{OL} = 4.0 mA			0.4	V
Input Pins < Input CMOS level schmitt trigger > MODE							
C62	Input high voltage	V_{IH9}		V_{DD}x0.9			V
C63	Input low voltage	V_{IL9}				V_{DD}x0.1	V
C64	Input leakage current	V_{LO9}	V_{DD} = 5.5 V V_I = V_{SS} to V_{DD}			±10	µA
Input Pins 2 < Input TTL level schmitt trigger > /NMI							
C65	Input high voltage	V_{IH10}		2.4			V
C66	Input low voltage	V_{IL10}				0.8	V
C67	Input leakage current	V_{LO10}	V_{DD} = 5.5 V V_I = V_{SS} to V_{DD}			±10	µA
OSCI pin, XI pin (at external clock input) : crystal, ceramic self-excited oscillation See Figure 1-4-2 to Figure 1-4-3							
C68	Input high voltage	V_{IH11}		V_{DD}x0.8		V_{DD}	V
C69	Input low voltage	V_{IL11}		V_{SS}		V_{DD}x0.2	V
Pin Capacitance							
C70	Input pin	C_{IN}	V_{IN} = 0 V Ta=25 C		7	15	pF
C71	Output pin	C_{OUT}			7	15	pF
C72	Input/output pin	$C_{I/O}$			7	15	pF

D. A/D Converter Characteristics

V_{DD} = 5.0 V
V_{SS} = 0 V
Ta = 25 C

Parameter		Symbol	Conditions		Capacitance			Unit
					Min	Typ	Max	
D1	Resolution						8	Bits
D2	A/D conversion relative precision		V_{DD} = 5 V	AN3-0			±3	LSB
			V_{SS} = 0 V	AN7-4			±4	LSB
D3	A/D conversion time		Fosc = 22.6 MHz		4.24			µs
D4	A/D conversion cycle		Fosc = 22.6 MHz		4.24			µs
D5	Analog input voltage	V_{IA}			V_{SS}		V_{DD}	V

E. AC Characteristics

Input Timing Conditions

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
External Clock Input Timing (Fosc1 = 22.6 MHz)							
E1	External clock input cycle time	t_{EXCcyc}	Fig 9-1	44.25			ns
E2	external clock input high pulse width	t_{EXCH}		$\frac{t_{EXCYC}}{2}$ -5			ns
E3	External clock input low pulse width	t_{EXCL}		$\frac{t_{EXCYC}}{2}$ -5			ns
E4	External clock input rise time	t_{EXCR}				5	ns
E5	External clock input fall time	t_{EXCF}				5	ns
Reset Input Timing							
E6	Reset signal pulse width (/RST)	t_{RSTW}	Fig 9-2	4			t_{EXCcyc}

Input Timing Conditions

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Data Transfer Signal Input Timing							
E7	Data acknowledge signal setup time (WAIT)	t_{WAITS}	Fig 9-4 Fig 9-6	20			ns
E8	Data acknowledge signal hold time (WAIT)	t_{WAITH}		0			ns
Data Transfer Signal Input Timing							
E9	Read data setup time (D15-00)	t_{RDS}	Fig 9-3 Fig 9-4 Fig 9-5 Fig 9-6	20			ns
E10	Read data hold time (D15-00)	t_{RDH}		0			ns
Bus Authority Request Input Timing							
E11	Bus authority request signal setup time (/BREQ)	t_{BREQS}	Fig 9-8	0			ns
E12	Bus authority request signal hold time (/BREQ)	t_{BREQH}		0			ns
Interrupt Signal Input Timing							
E13	Nonmaskable interrupt signal pulse width (NMI)	t_{NMIW}	Fig 9-9	5 (Note)			t_{cyc}
E14	External interrupt signal pulse width (/IRQ4-0)	t_{IRQW}		2 (Note)			t_{cyc}

Note : An interrupt may occur when the noise of the specified time or less is input.

Input Timing Conditions

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C

	Parameter	Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Serial Interface Related Signal Timing (Synchronous Serial Reception)							
E15	Data reception setup time (SBI1-0)	t_{RXDS}	Fig 9-13	25			ns
E16	Data reception hold time (SBI1-0)	t_{RXDH}		25			ns
E17	Serial clock input high pulse width (SBT1-0)	t_{SCH}		tcyc+100			ns
E18	Serial clock input low pulse width (SBT1-0)	t_{SCL}		tcyc+100			ns
Timer/Counter Signal Input Timing							
E19	Timer external input clock low pulse width (TMnIO: n=5-0) (TMnIOA, TMnIOB, TMnIC: n=6,7)	t_{TCCLKL}	Fig 9-14	t_{cyc}			ns
E20	Timer external input clock high pulse width (TMnIO: n=5-0) (TMnIOA, TMnIOB, TMnIC: n=6,7)	t_{TCCLKH}		t_{cyc}			ns

F. AC Characteristics (Output)

Output Signal Characteristics

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C
C_L = 70 pF

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
System Clock Output Timing							
F1	System clock output cycle time (SYSCLK)	t_{cyc}	Fig 9-1	88.5			ns
F2	System clock output low pulse width (SYSCLK)	t_{CL}		39.25			ns
F3	System clock output high pulse width (SYSCLK)	t_{CH}		29.25			ns
F4	System clock output rise time (SYSCLK)	t_{CR}				10	ns
F5	System clock output fall time (SYSCLK)	t_{CF}				10	ns

Output Signal Characteristics

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C
C_L = 70 pF

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Data Transfer Signal Output Timing 1							
F6	Address delay time 1 (A23-0), (A23-16)	t_{AD1}	Fig 9-3 to Fig 9-6			30	ns
F7	Address delay time 2 (AD15-0)	t_{AD2}	Fig 9-5 Fig 9-6	$\frac{tcyc}{4}$		$\frac{tcyc}{4}+15$	ns
F8	Address hold time 1 (A23-0), (A23-16)	t_{AH1}	Fig 9-3 Fig 9-4	5			ns
F9	Address hold time 2 (A23-0), (A23-16)	t_{AH2}	Fig 9-5 Fig 9-6	$\frac{tcyc}{4}$			ns
F10	Address hold time 3 (AD15-0)	t_{AH3}	Fig 9-5 Fig 9-6	$\frac{tcyc}{4}-10$			ns
F11	Address/Data hold time 1 (AD15-0)	t_{ADH1}		5			ns
F12	Address/Data hold time 2 (AD15-0)	t_{ADH2}		$\frac{tcyc}{4}$			ns
F13	Data delay time 1 (D15-0)	t_{DD1}	Fig 9-3 Fig 9-4			15	ns
F14	Data delay time 2 (AD15-0)	t_{DD2}	Fig 9-5 Fig 9-6			$\frac{tcyc}{2}$	ns
F15	Data delay time 3 (D15-0)	t_{DD3}	Fig 9-7	$\frac{tcyc}{4}$			ns
F16	Data hold time 1 (D15-0)	t_{DH1}	Fig 9-3 Fig 9-4	5			ns
F17	Data hold time 2 (D15-0)	t_{DH2}		$\frac{tcyc}{4}$			

Output Signal Characteristics

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C
C_L = 70 pF

Parameter		Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Data Transfer Signal Output Timing 2							
F18	Chip-select signal fall delay time 1 (/CS3-0), (/CS3-1)	t_{CSDF1}	Fig 9-3 to Fig 9-7			20	ns
F19	Chip-select signal rise delay time 1 (/CS3-0), (/CS3-1)	t_{CSDR1}				20	ns
F20	Chip-select signal fall delay time 2 (/CS0)	t_{CSDF2}	Fig 9-7			$\frac{t_{CYC}}{4}$ +10	ns
F21	Chip-select signal rise delay time 2 (/CS0)	t_{CSDR2}				$\frac{t_{CYC}}{4}$ +10	ns
F22	Chip-select signal hold time 1 (/CS3-0)	t_{CSH1}	Fig 9-3 Fig 9-4 Fig 9-5 Fig 9-6	5			ns
F23	Chip-select signal hold time 2 (/CS3-0)	t_{CSH2}		$\frac{t_{CYC}}{4}$			ns
F24	Address latch signal fall delay time (ALE)	t_{ALEDF}	Fig 9-5 Fig 9-6	$\frac{t_{CYC}}{4}$ -10			ns
F25	Address latch signal pulse width (ALE)	t_{ALEPW}		$\frac{t_{CYC}}{2}$ -10			ns
F26	Address latch signal hold time 1 (ALE)	t_{ALEH1}		5			ns
F27	Address latch signal hold time 2 (ALE)	t_{ALEH2}		$\frac{t_{CYC}}{4}$			ns

Output Signal Characteristics

V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C
C_L = 70 pF

	Parameter	Symbol	Conditions	Capacitance			Unit
				Min	Typ	Max	
Data Transfer Signal Output Timing 3							
F28	Read enable signal fall delay time 1 (/RE)	t_{REDF1}	Fig 9-3 Fig 9-4			10	ns
F29	Read enable signal fall delay time 2 (/RE)	t_{REDF2}	Fig 9-5 Fig 9-6			15	ns
F30	Read enable signal fall delay time 3 (/RE)	t_{REDF3}	Fig 9-7			20	ns
F31	Read enable signal rise delay time 1 (/RE)	t_{REDR1}	Fig 9-3 to Fig 9-6			15	ns
F32	Read enable signal rise delay time 2 (/RE)	t_{REDR2}	Fig 9-7			$\frac{tcyc}{4}$+10	ns
F33	Read enable signal hold time (/RE)	t_{REH}		$\frac{tcyc}{4}$			ns
F34	Burst ROM read enable signal fall delay time (/BSTRE)	t_{BREDF}				20	ns
F35	Burst ROM read enable signal fall delay time (/BSTRE)	t_{BREDR}				$\frac{tcyc}{4}$+10	ns
F36	Read enable signal pulse width time 1 (/RE)	t_{REPW1}	Fig 9-3 Fig 9-4	$\frac{tcyc}{2}$-20	*		ns
F37	Read enable signal pulse width time 2 (/RE)	t_{REPW2}		$\frac{tcyc}{2}$-20	*		ns
F38	Read enable signal pulse width time 3 (/RE)	t_{REPW1}	Fig 9-5 Fig 9-6	tcyc-10	*		ns
F39	Read enable signal pulse width time 4 (/RE)	t_{REPW3}		$\frac{3}{4}$x tcyc -10	*		ns
F40	Write enable signal fall delay time 1 (/WEH, WEL)	t_{WEDF4}	Fig 9-3 Fig 9-4			15	ns
F41	Write enable signal fall delay time 2 (/WEH, WEL)	t_{WEDF2}	Fig 9-5 Fig 9-6			20	ns
F42	Write enable signal fall delay time 3 (/WEH, WEL)	t_{WEDF3}	Fig 9-7	$\frac{tcyc}{4}$			ns
F43	Write enable pulse width time 1 (/WEH, WEL)	t_{WEPW1}	Fig 9-3 Fig 9-4	$\frac{tcyc}{2}$-20	*		ns
F44	Write enable pulse width time 2 (/WEH, WEL)	t_{WEPW2}		$\frac{tcyc}{4}$-20	*		ns
F45	Write enable pulse width time 3 (/WEH, WEL)	t_{WEPW3}	Fig 9-5 Fig 9-6	tcyc-10	*		ns
F46	Write enable pulse width time 4 (/WEH, WEL)	t_{WEPW4}		$\frac{3}{4}$x tcyc -10	*		ns

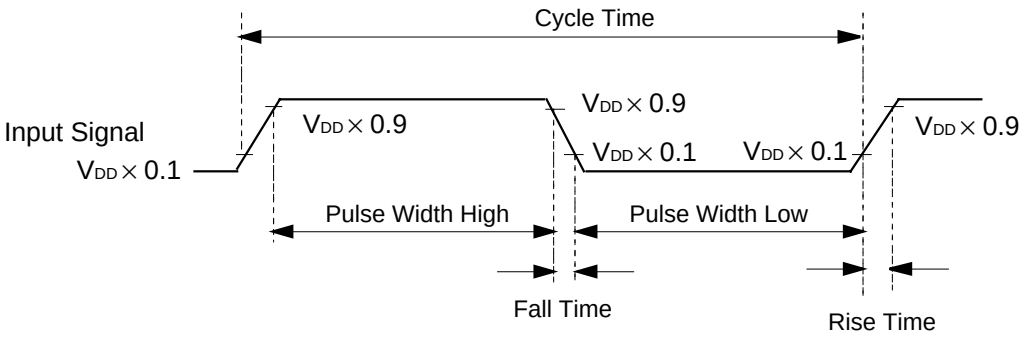
* is standaard value in no wait cycle. It is (listed value)+N*tCYC in N wait cycle.

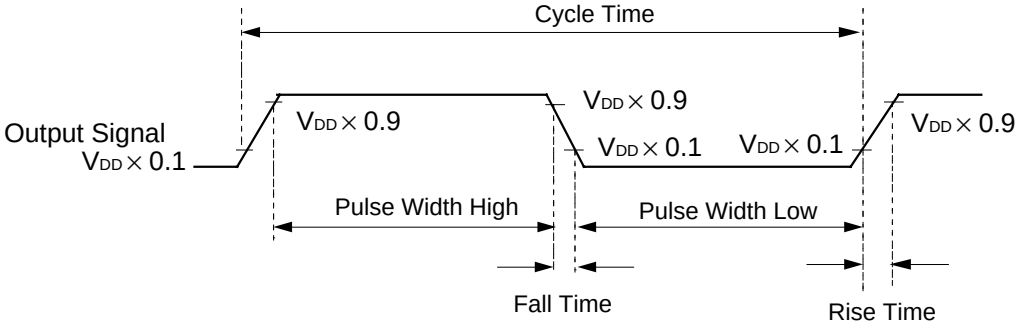
Output Signal Characteristics

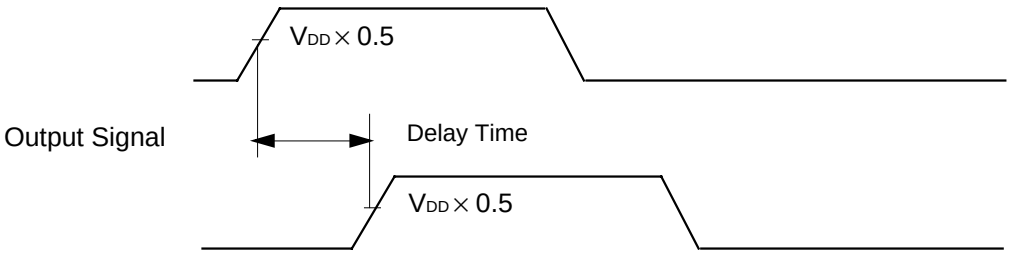
V_{DD} = 4.5 V to 5.5 V
V_{SS} = 0 V
Ta = -40 C to +85 C
C_L = 70 pF

Parameter		Symbol	Conditions		Capacitance			Unit
					Min	Typ	Max	
Serial Interface Signal Output Timing (Synchronous Serial Transmission)								
F47	Transfer data delay time (SBO1-0)	t_{TXDD}	Fig 9-10 Fig 9-11 Fig 9-12	Normal			$\frac{tcyc}{2}$	ns
				I2C			t_{cyc}x2	ns
F48	Transfer data hold time (transfer in progress) (SBO1-0)	t_{TXDH1}	Fig 9-10		10			ns
F49	Transfer data hold time (Transfer end timing at SBT input) (SBO1-0)	t_{TXDH2}	Fig 9-11		$\frac{tcyc}{2}$			ns
F50	Transfer data hold time (Transfer end timing at SBT output) (SBO1-0)	t_{TXDH3}	Fig 9-12		$\frac{t_{SCH}+t_{SCL}}{2}$			ns

AC Timing Voltage Level







(Both setup time and hold time are $V_{DD} \times 0.5$)

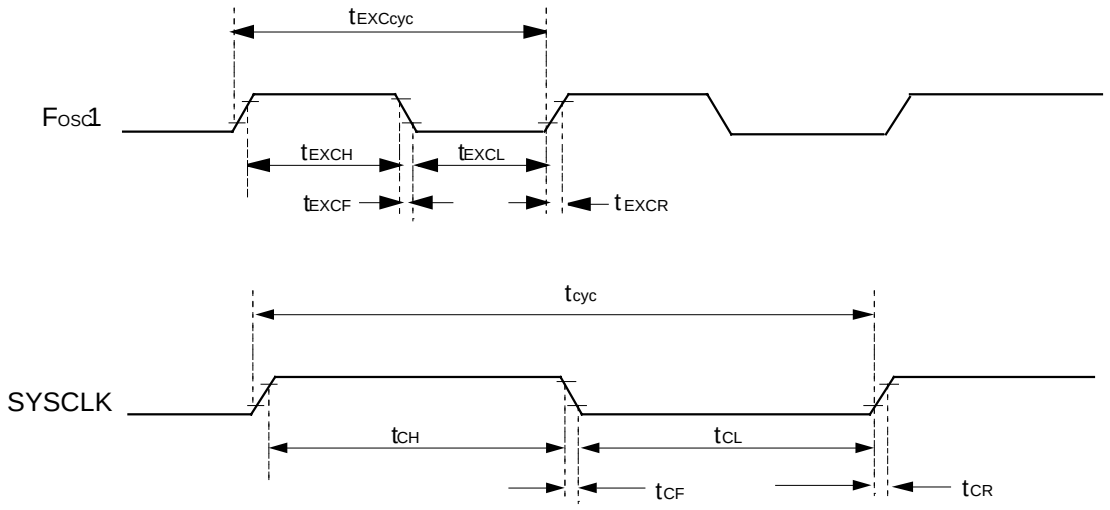


Fig. 9-1-1 System Clock Timing

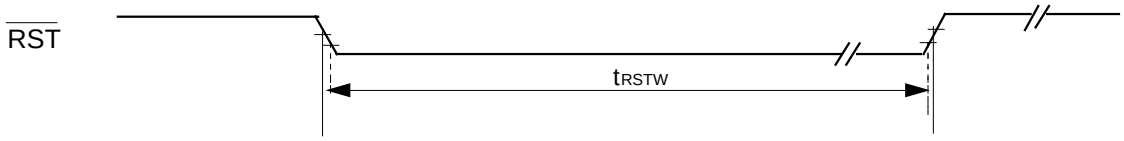


Fig. 9-1-2 Reset Timing

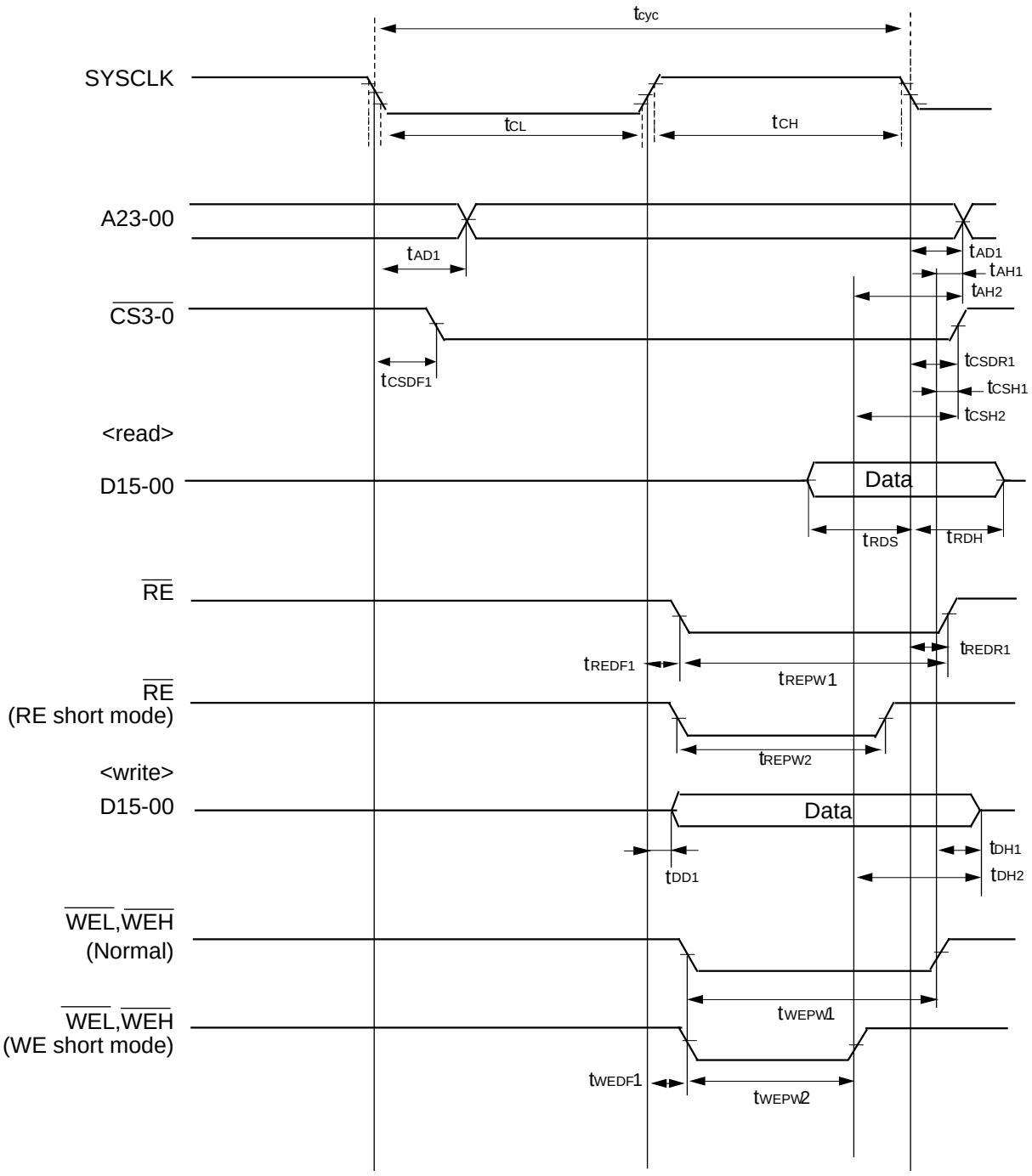


Fig. 9-1-3 Data Transfer Signal Timing (Address/Data Separate Mode, Without Wait)

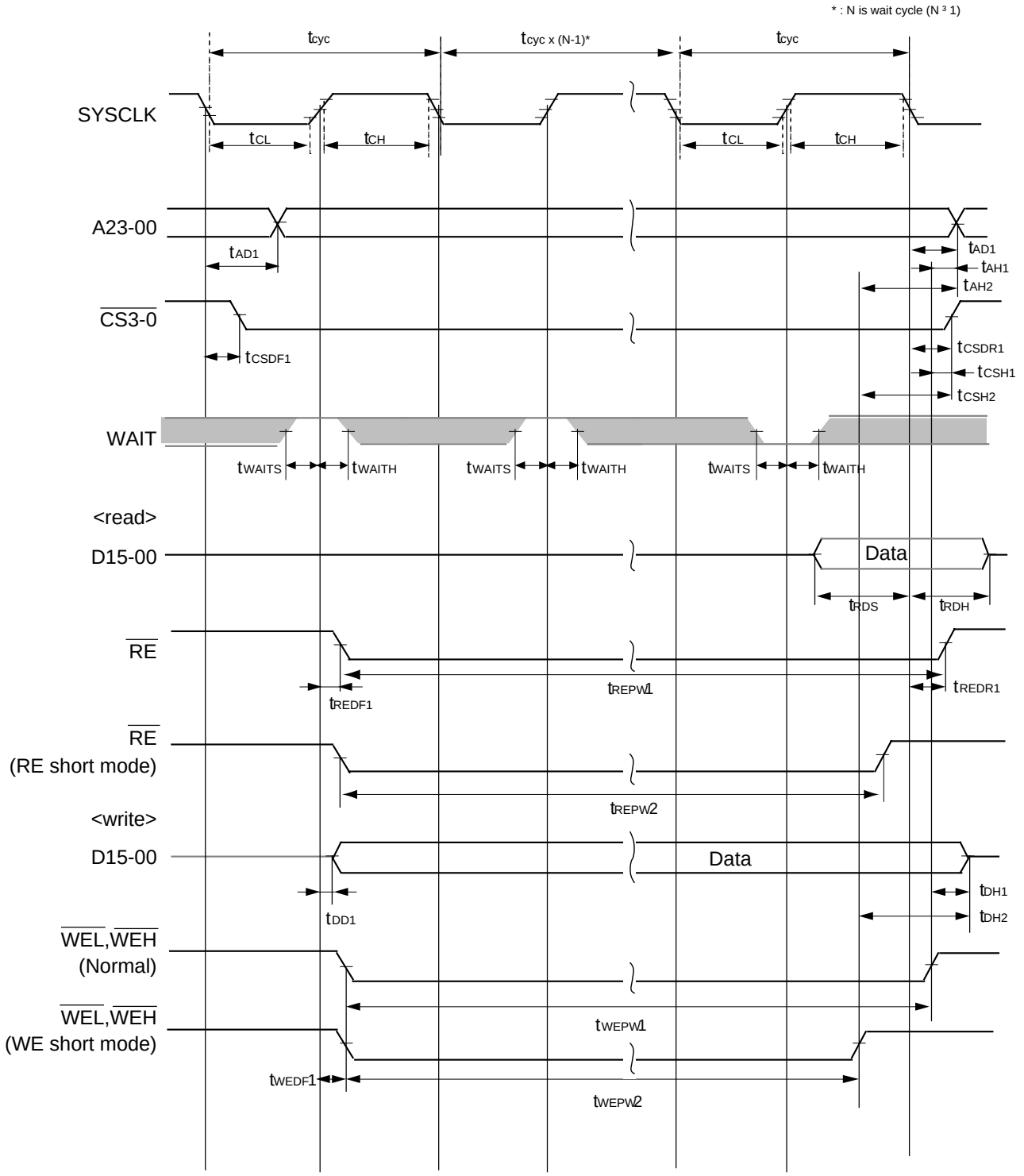


Fig. 9-1-4 Data Transfer Signal Timing (Address/Data Separate Mode, With Wait)

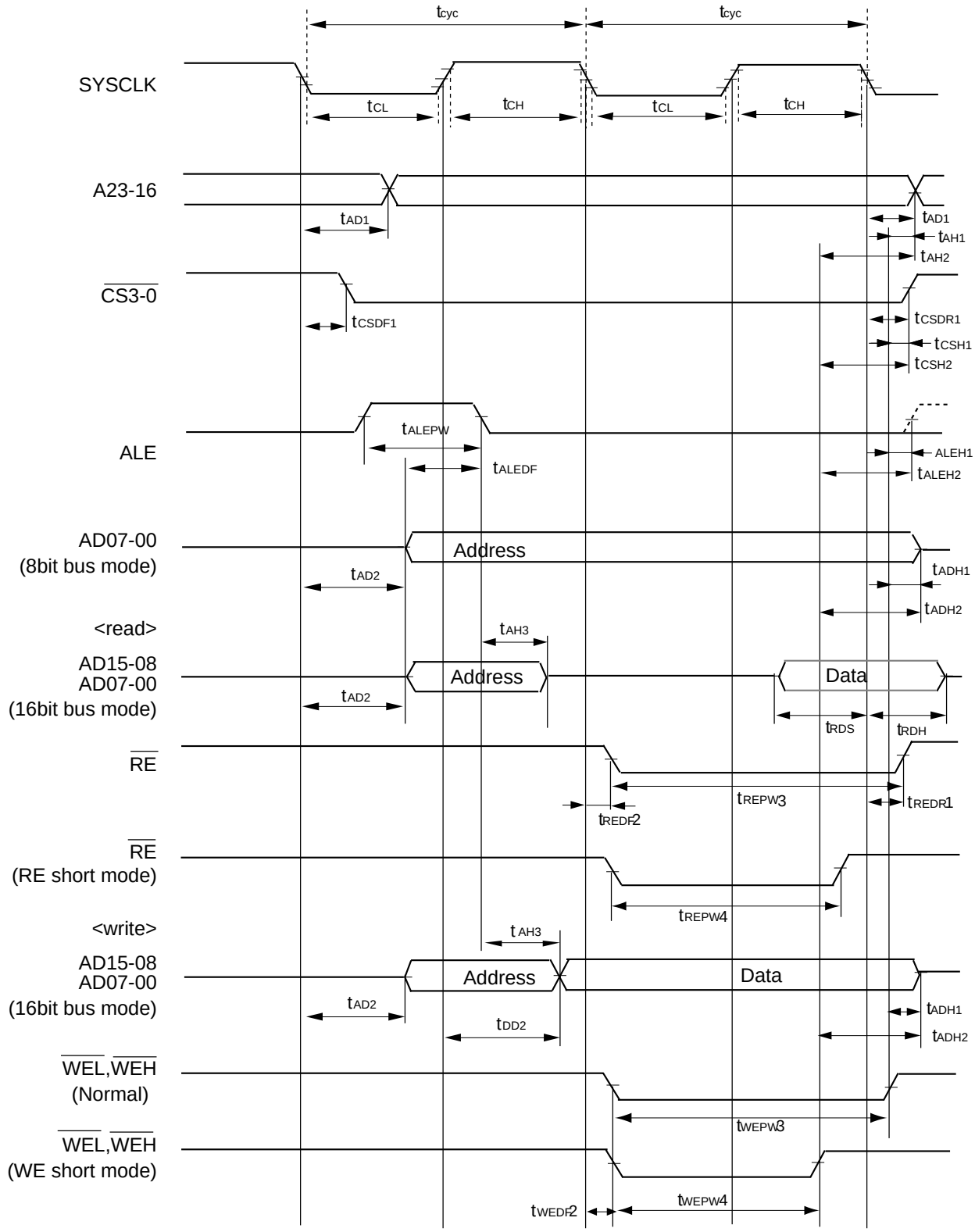


Fig. 9-1-5 Data Transfer Signal Timing (Address/Data Share Mode, Without Wait)

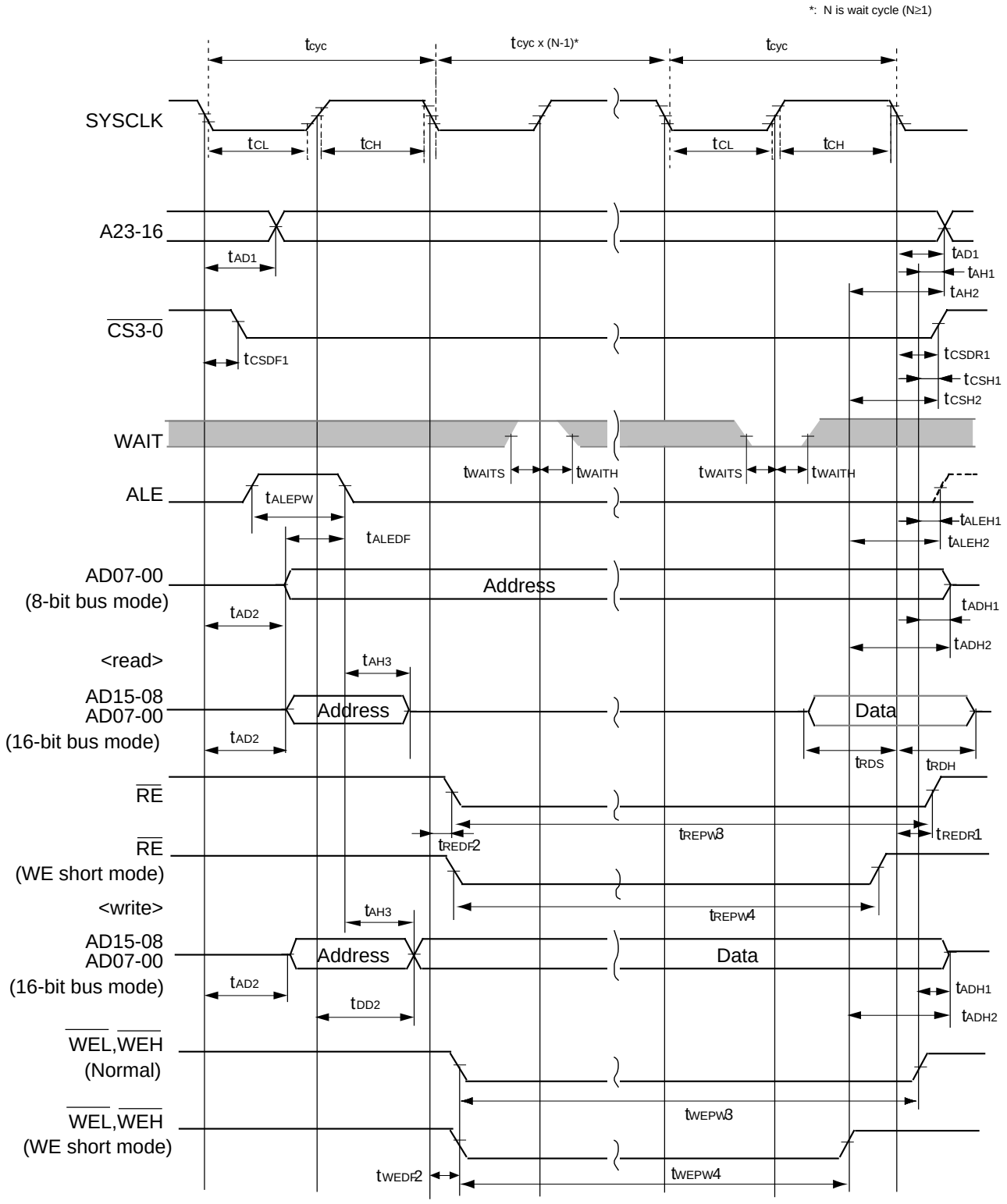


Fig. 9-1-6 Data Transfer Signal Timing (Address/Data Share Mode, With Wait)

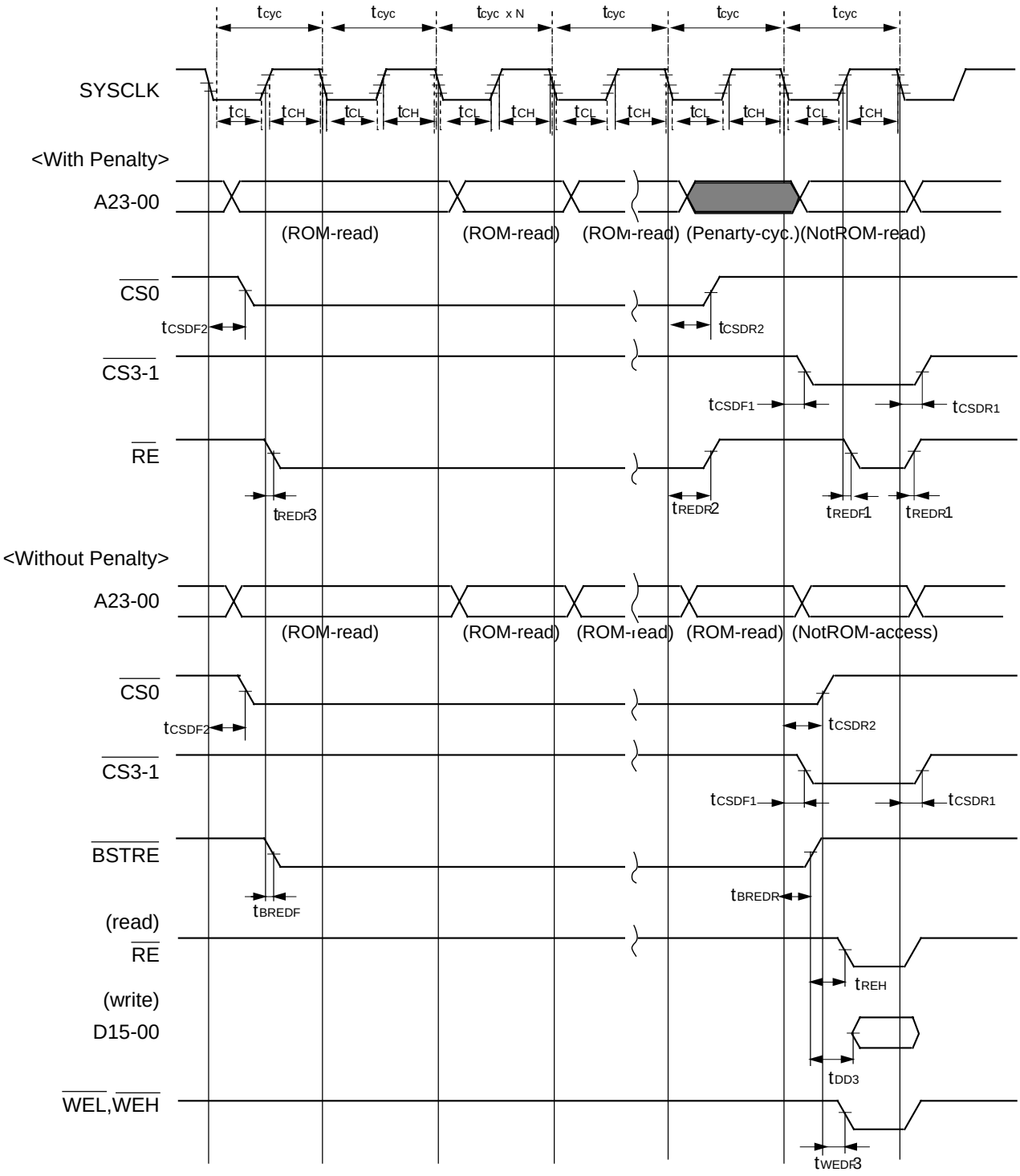


Fig. 9-1-7 Data Transfer Signal Timing (Burst ROM Interface)

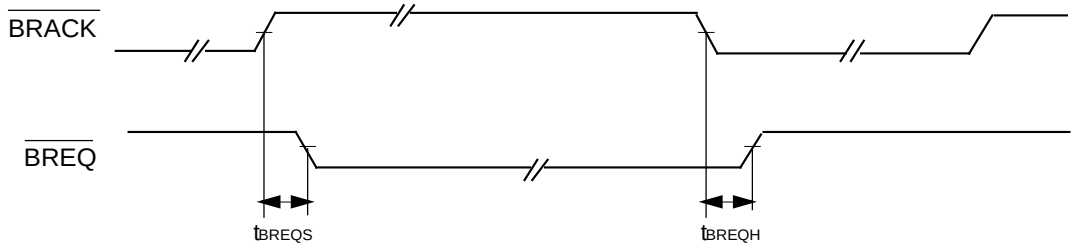


Fig. 9-1-8 Bus Authority Request Signal Timing

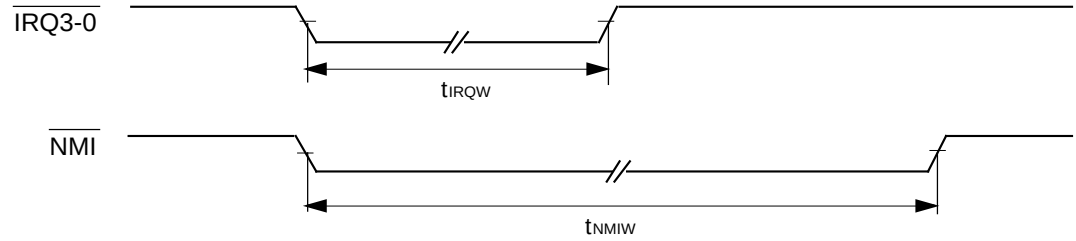


Fig. 9-1-9 Interrupt Signal Timing

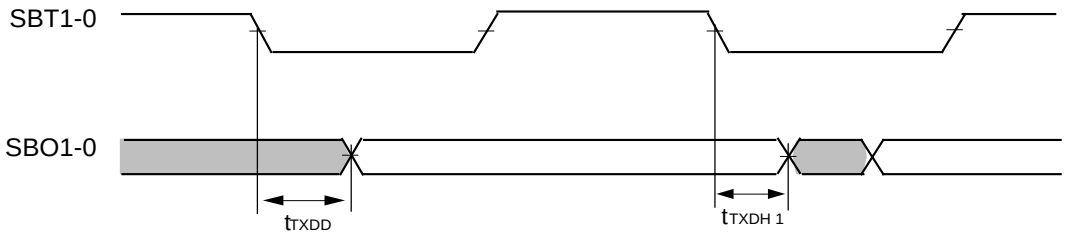


Fig. 9-1-10 Serial Interface Signal Timing 1
(Synchronous Serial Transmission: Transfer in Progress)

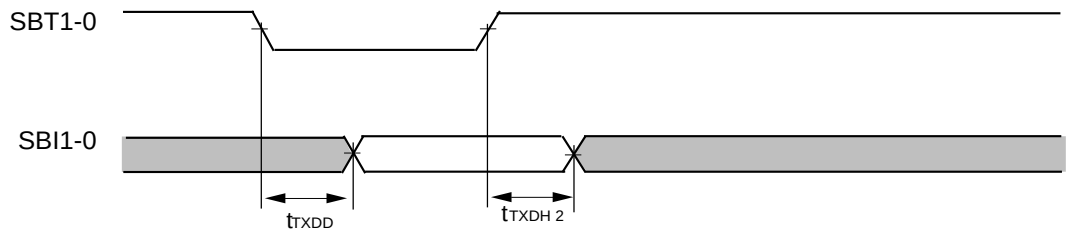


Fig. 9-1-11 Serial Interface Signal Timing 2
(Synchronous Serial Transmission: Transfer End Timing at SBT Input)

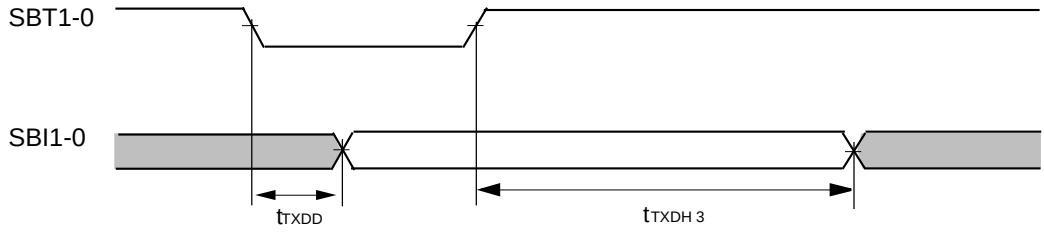


Fig. 9-1-12 Serial Interface Signal Timing 3
(Synchronous Serial Transmission: Transfer End Timing at SBT Output)

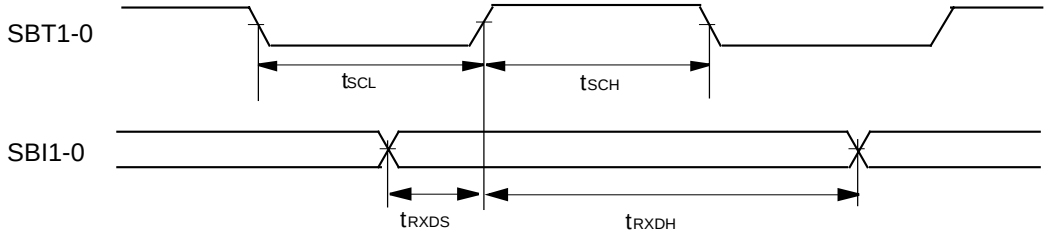


Fig. 9-1-13 Serial Interface Signal Timing 2
(Synchronous Serial Reception)

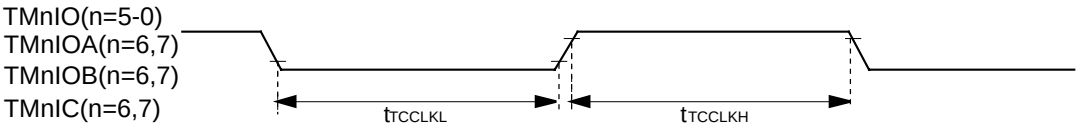


Fig. 9-1-14 Timer/Counter Signal Timing

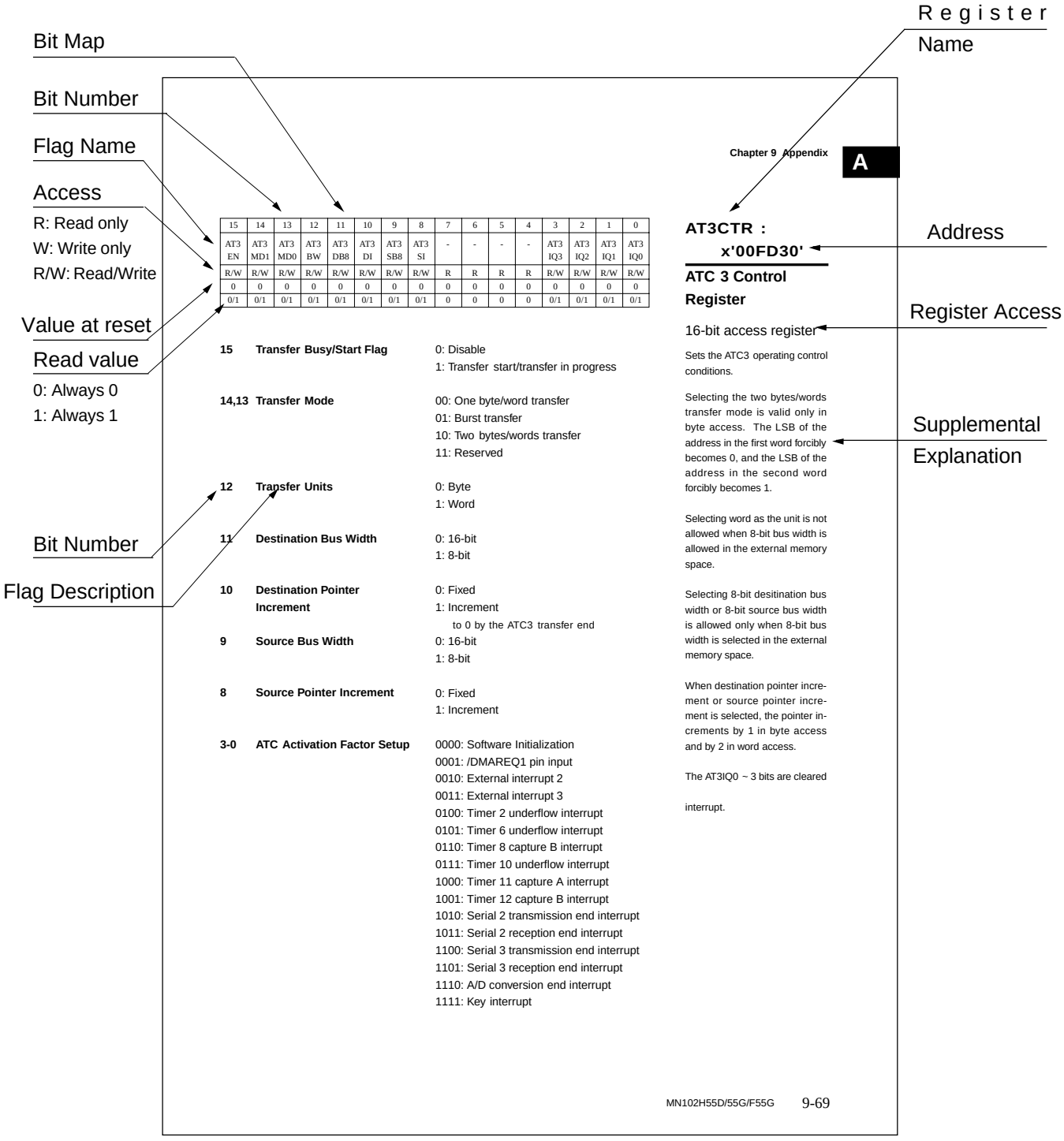
9-2 Data Appendix

9-2-1 List of Special Registers

About This Section

■ Description of Each Page

Each page of this chapter describes one or more registers. Each page lists the register name, address, register access, bit map, flag explanation of each bit number and supplementary explanation. The following is the layout and definition of this section.


Register Name
Bit Map
Bit Number
Flag Name
Access
R: Read only
W: Write only
R/W: Read/Write
Value at reset
Read value
0: Always 0
1: Always 1
Bit Number
Flag Description
Address
Register Access
Supplemental Explanation
Chapter 9 Appendix
A
AT3CTR : x'00FD30'
ATC 3 Control Register
16-bit access register
Sets the ATC3 operating control conditions.
Selecting the two bytes/words transfer mode is valid only in byte access. The LSB of the address in the first word forcibly becomes 0, and the LSB of the address in the second word forcibly becomes 1.
Selecting word as the unit is not allowed when 8-bit bus width is allowed in the external memory space.
Selecting 8-bit desitination bus width or 8-bit source bus width is allowed only when 8-bit bus width is selected in the external memory space.
When destination pointer increment or source pointer increment is selected, the pointer increments by 1 in byte access and by 2 in word access.
The AT3IQ0 ~ 3 bits are cleared
interrupt.
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
AT3EN AT3MD1 AT3MD0 AT3BW AT3DB8 AT3DI AT3SB8 AT3SI - - - - AT3IQ3 AT3IQ2 AT3IQ1 AT3IQ0
R/W R/W R/W R/W R/W R/W R/W R/W R R R R R/W R/W R/W R/W
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0/1 0/1 0/1 0/1 0/1 0/1 0/1 0/1 0 0 0 0 0/1 0/1 0/1 0/1
15 Transfer Busy/Start Flag
0: Disable
1: Transfer start/transfer in progress
14,13 Transfer Mode
00: One byte/word transfer
01: Burst transfer
10: Two bytes/words transfer
11: Reserved
12 Transfer Units
0: Byte
1: Word
11 Destination Bus Width
0: 16-bit
1: 8-bit
10 Destination Pointer Increment
0: Fixed
1: Increment
to 0 by the ATC3 transfer end
9 Source Bus Width
0: 16-bit
1: 8-bit
8 Source Pointer Increment
0: Fixed
1: Increment
3-0 ATC Activation Factor Setup
0000: Software Initialization
0001: /DMAREQ1 pin input
0010: External interrupt 2
0011: External interrupt 3
0100: Timer 2 underflow interrupt
0101: Timer 6 underflow interrupt
0110: Timer 8 capture B interrupt
0111: Timer 10 underflow interrupt
1000: Timer 11 capture A interrupt
1001: Timer 12 capture B interrupt
1010: Serial 2 transmission end interrupt
1011: Serial 2 reception end interrupt
1100: Serial 3 transmission end interrupt
1101: Serial 3 reception end interrupt
1110: A/D conversion end interrupt
1111: Key interrupt
MN102H55D/55G/F55G 9-69

C

CPUM : x'00FC00'

CPU Mode Control Register

16-bit access register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD RST	WD lng1	WD lng0	-	-	-	-	-	-	-	-	OSC ID	STOP	HALT	OSC1	OSC0
R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
1	0	0	0	0	1	1	1	0	0	1	1	0	1	1	1
0/1	0/1	0/1	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1

15 **Watchdog Timer Enable** 0: Enable 1: Disable and clear

Setting WDRST to '0' after setting it to '1' clears the watchdog timer counting value and starts counting. The watchdog timer consists of a 17-bit binary counter counting on the oscillation clock. Therefore, clear the watchdog timer counting value within 2^{16} (65,536) machine cycles.

14:13 **Watchdog Timer Count *** 00: 2^{16}
01: 2^{4}
10: 2^{8}
11: Reserved

4 **System Clock Monitor** 0: High-speed
1: Low-speed

Changing the set value reduces the wait time for oscillation stabilization when returning from STOP mode. (At reset release, the wait time for oscillation stabilization is 2^{16} (65,536) machine cycles.

3 **CPU Operating Control (STOP tranfer request)** 0000: NORMAL mode
0001: IDLE mode
0011: SLOW mode

2 **CPU Operating Control (HALT tranfer request)** 0100: HALT0 mode
0111: HALT1 mode
1000: STOP0 mode
1011: STOP1 mode

1:0 **Oscillator Control**

The following describes programming rules and precautions in the STOP/HALT mode.

Points for Programming

(1) Setting the CPUM address in the address register in advance, set the CPUM register using the MOV instruction with the register indirect addressing mode.
(2) Immediately after the MOV instruction, locate three NOPs consecutively.
(3) Immediately before the MOV instruction, locate the JMP instruction and align to the even address. This avoids the effects by the differences of the bus widths in the memory mode or expansion mode and provides the same result when operating in any conditions.

Programming Coding Example in Assembler (as 102Ver.1.0, Ver.2.0)

```
        MOV     CPUM, A0    ; Set A0 to the CPUM address.
        MOV     (A0), D0    ; Transfer the contents of CPUM to D0.
        OR      x'000*', D0 ; Generate the data to set the STOP/HALT mode.
        JMP     STP_HLT     ; Branch unconditionally to the even address to
        ALIGN   2           ; eliminate the difference of operating conditions.
STP_HLT MOV     D0, (A0)    ; Set the STOP/HALT mode to CPUM.
        NOP                 ; Dummy
        NOP                 ; Dummy
        NOP                 ; Dummy
```

Precautions

(1) * of OR instruction varies depending on the STOP or HALT mode.
(2) Set the ALIGN value to '2' or more in the above file when the ALIGN value is set using SECTION dummy instruction before this programming coding is described.
(3) Code the above programming in another file of the assembler source file when the program is developed with C complier cc 102.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	HSWT IOE	NWAIT IOE	WAIT SET	ARB SZ	-	WAIT IO1	WAIT IO0	-	WAIT 2	WAIT 1	WAIT 0
R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	1	1	1	0	0	1	1	0	1	1	1
0	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0	0/1	0/1	0/1

MEMCTR : x'00FC02'

Memory Control Register

16-bit access register

In this series, set MEMCTR to x'0410' or x'0490'.

10 **Peripheral Fixed Wait Cycle Enable Flag During Handshake Mode**
0: No Wait
1: Peripheral Fixed Wait Cycle
(Always set '1' in this series.)

9 **Peripheral Fixed Wait Cycle Enable Flag**
0: Enable 1: Disable
(Always set '0' in this series.)

8 **Fixed Wait Mode/ Handhsake Mode Switch**
0: Handshake Mode
1: Fixed Wait Mode
(Always set '0' in this series.)

7 **Bus Width Setup Flag for Fixed Area (x'040000' to x'07FFFF')**
0: Based on $\overline{\text{WORD}}$ pin
1: 8-bit Bus Access regardless of $\overline{\text{WORD}}$ pin

5:4 **Peripheral Fixed Wait Cycle**
00: No wait
01: 1 wait cycle
10: 2 wait cycles
11: 3 wait cycles
(Always set '01' in this series.)

2:0 **Fixed Wait Cycle**
000: No wait cycle
001: 1 wait cycle
010: 2 wait cycles
011: 3 wait cycles
100: 4 wait cycles
101: 5 wait cycles
110: 6 wait cycles
111: 7 wait cycles
(Don't care in this series.)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	GN4	GN3	GN2	GN1	GN0	-
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0

IAGR : x'00FC0E'

Interrupt Accept Group Register

8/16-bit access register

IAGR is a read-only register.

5:1 Group Number of Accepted Interrupt

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	WAIT 1	WAIT 0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1

MEMMD0 : x'00FC30'

Memory Mode Control Register 0

16-bit access register

Set any values when block 0 is unused.

1:0 Wait Cycle for Block 0

00: No Wait
01: 1 Wait Cycle
10: 2 Wait Cycles
11: Handshake

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESHT	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT 1	WAIT 0
R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0	0	0	0	0	0	0/1	0	0	0	0	0	0	0/1	0/1

MEMMD1 : x'00FC32'

Memory Mode Control Register 1

16-bit access register

Set any values when block 1 is unused.

15 **Block 1 $\overline{RE}$ pulse width shortening**
0: Disable
1: Enable

8 **Bus Mode for Block 1**
0: 16-bit Bus Mode
1: 8-bit Bus Mode

1:0 **Wait Cycle for Block 1**
00: No Wait
01: 1 Wait Cycle
10: 2 Wait Cycles
11: Handshake

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESHT	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT 1	WAIT 0
R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0	0	0	0	0	0	0/1	0	0	0	0	0	0	0/1	0/1

MEMMD2 : x'00FC34'

Memory Mode Control Register 2

16-bit access register

Set any values when block 2 is unused.

15 **Block 2 $\overline{RE}$ pulse width shortening**
0: Disable
1: Enable

8 **Bus Mode for Block 2**
0: 16-bit Bus Mode
1: 8-bit Bus Mode
(Select the same bus width as the bus width set by $\overline{WORD}$ pin.)

1:0 **Wait Cycle for Block 2**
00: No Wait
01: 1 Wait Cycle
10: 2 Wait Cycles
11: Handshake

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESHT	-	-	-	-	-	-	BMOD	-	-	-	-	-	-	WAIT 1	WAIT 0
R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0	0	0	0	0	0	0/1	0	0	0	0	0	0	0/1	0/1

MEMMD3 : x'00FC36'

Memory Mode Control Register 3

16-bit access register

Set any values when block 3 is unused.

15 **Block 3 $\overline{RE}$ pulse width shortening**
0: Disable
1: Enable

8 **Bus Mode for Block 3**
0: 16-bit Bus Mode
1: 8-bit Bus Mode

1:0 **Wait Cycle for Block 3**
00: No Wait
01: 1 Wait Cycle
10: 2 Wait Cycles
11: Handshake

M

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	UNIF	WDIF	NMIF
R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

G0ICR : x'00FC40'

Nonmaskable Interrupt Control Register 0

8/16-bit access register

2 **Nonmaskable Interrupt Request Flag by Executing Undefined Instruction**
0: No interrupt requested
1: Interrupt requested

1 **Nonmaskable Interrupt Request Flag by Overflowing Watchdog Timer**
0: No interrupt requested
1: Interrupt requested

0 **Nonmaskable Interrupt Request Flag by $\overline{NMI}$ Pin**
0: No interrupt requested
1: Interrupt requested

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G1 LV2	G1 LV1	G1 LV0	-	TM5 IE	TM0 IE	IRQ0 IE	-	TM5 IR	TM0 IR	IRQ0 IR	-	TM5 ID	TM0 ID	IRQ0 ID
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1

G1ICR : x'00FC42'

Maskable Interrupt Control Register 1

8/16-bit access register

14:12 Group 1 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

10 Timer 5 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

9 Timer 0 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

8 IRQ0 Interrupt Enable Flag — 0: Disable 1: Enable

6 Timer 5 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when timer 5 underflows.

5 Timer 0 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when timer 0 underflows.

4 IRQ0 Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when an external interrupt occurs from IRQ0 pin.

2 Timer 5 Underflow Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

1 Timer 0 Underflow Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

0 IRQ0 Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G2 LV2	G2 LV1	G2 LV0	-	AN IE	TM1 IE	IRQ1 IE	-	AN IR	TM1 IR	IRQ1 IR	-	AN ID	TM1 ID	IRQ1 ID
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1

G2ICR : x'00FC44'

Maskable Interrupt Control Register 2

8/16-bit access register

14:12 Group 2 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

10 A/D Conversion End Interrupt Enable Flag — 0: Disable 1: Enable

9 Timer 1 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

8 IRQ1 Interrupt Enable Flag — 0: Disable 1: Enable

6 A/D Conversion End Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when the A/D conversion ends.

5 Timer 1 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when timer 1 underflows.

4 IRQ1 Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when an external interrupt occurs from IRQ1 pin.

2 A/D Conversion End Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

1 Timer 1 Underflow Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

0 IRQ1 Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G3 LV2	G3 LV1	G3 LV0	SC0R IE	SC0T IE	TM2 IE	IRQ2 IE	SC0R IR	SC0T IR	TM2 IR	IRQ2 IR	SC0R ID	SC0T ID	TM2 ID	IRQ2 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1

G3ICR : x'00FC46'

Maskable Interrupt Control Register 3

8/16-bit access register

14:12 Group 3 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

11 Serial 0 Reception End Interrupt Enable Flag — 0: Disable 1: Enable

10 Serial 0 Transmission End Interrupt Enable Flag — 0: Disable 1: Enable

9 Timer 2 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

8 IRQ2 Interrupt Enable Flag — 0: Disable 1: Enable

7 Serial 0 Reception End Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when the serial 0 reception ends.

6 Serial 0 Transmission End Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when the serial 0 transmission ends.

5 Timer 2 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when timer 2 underflows.

4 IRQ2 Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when an external interrupt occurs from IRQ2 pin.

3 Serial 0 Reception End Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

2 Serial 0 Transmission End Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

1 Timer 2 Underflow Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

0 IRQ2 Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G4 LV2	G4 LV1	G4 LV0	SC1R IE	SC1T IE	TM3 IE	IRQ3 IE	SC1R IR	SC1T IR	TM3 IR	IRQ3 IR	SC1R ID	SC1T ID	TM3 ID	IRQ3 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

G4ICR : x'00FC48'

Maskable Interrupt Control Register 4

8/16-bit access register

14:12 Group 4 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

11 Serial 1 Reception End Interrupt Enable Flag — 0: Disable 1: Enable

10 Serial 1 Transmission End Interrupt Enable Flag — 0: Disable 1: Enable

9 Timer 3 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

8 IRQ3 Interrupt Enable Flag — 0: Disable 1: Enable

7 Serial 1 Reception End Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when the serial 1 reception ends.

6 Serial 1 Transmission End Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when the serial 1 transmission ends.

5 Timer 3 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when timer 3 underflows.

4 IRQ3 Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when an external interrupt occurs from IRQ3 pin.

3 Serial 1 Reception End Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

2 Serial 1 Transmission End Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

1 Timer 3 Underflow Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

0 IRQ3 Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G5 LV2	G5 LV1	G5 LV0	*Note	*Note	TM4 IE	IRQ4 IE	*Note	*Note	TM4 IR	IRQ4 IR	-	-	TM4 ID	IRQ4 ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1

*Note: Always set 0.

G5ICR : x'00FC4A'

Maskable Interrupt Control Register 5

8/16-bit access register

14:12 Group 5 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

9 Timer 4 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

8 IRQ4 Interrupt Enable Flag — 0: Disable 1: Enable

5 Timer 4 Underflow Interrupt Request Flag — 0: No interrupt requested; 1: Interrupt requested

Set '1' when timer 4 underflows.

4 IRQ4 Interrupt Request Flag — 0: No interrupt requested; 1: Interrupt requested

Set '1' when an external interrupt occurs from IRQ4 pin.

1 Timer 4 Underflow Interrupt Detect Flag — 0: No interrupt detected; 1: Interrupt detected

0 IRQ4 Interrupt Detect Flag — 0: No interrupt detected; 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G6 LV2	G6 LV1	G6 LV0	ATC IE	TM6B IE	TM6A IE	TM6U IE	ATC IR	TM6B IR	TM6A IR	TM6U IR	ATC ID	TM6B ID	TM6A ID	TM6U ID
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

G6ICR : x'00FC4C'

Maskable Interrupt Control Register 6

8/16-bit access register

14:12 Group 6 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

11 ATC Transfer End Interrupt Enable Flag — 0: Disable 1: Enable

10 Timer 6 Compare/Capture Interrupt B Enable Flag — 0: Disable 1: Enable

9 Timer 6 Compare/Capture Interrupt A Enable Flag — 0: Disable 1: Enable

8 Timer 6 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

Set '1' when ATC transfer ends. Set '1' when a timer 6 underflow interrupt or compare/capture interrupt occurs.

7 ATC Transfer End Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

6 Timer 6 Compare/Capture Interrupt B Request Flag — 0: No interrupt requested 1: Interrupt requested

5 Timer 6 Compare/Capture Interrupt A Request Flag — 0: No interrupt requested 1: Interrupt requested

4 Timer 6 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

3 ATC Transfer End Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

2 Timer 6 Compare/Capture Interrupt B Detect Flag — 0: No interrupt detected 1: Interrupt detected

1 Timer 6 Compare/Capture Interrupt A Detect Flag — 0: No interrupt detected 1: Interrupt detected

0 Timer 6 Underflow Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	G7 LV2	G7 LV1	G7 LV0	-	TM7B IE	TM7A IE	TM7U IE	-	TM7B IR	TM7A IR	TM7U IR	-	TM7B ID	TM7A ID	TM7U ID
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	0/1

G7ICR : x'00FC4E'

Maskable Interrupt Control Register 7

8/16-bit access register

14:12 Group 7 Interrupt Priority Level — 000 (level 0) to 110 (level 6)

10 Timer 7 Compare/Capture Interrupt B Enable Flag — 0: Disable 1: Enable

9 Timer 7 Compare/Capture Interrupt A Enable Flag — 0: Disable 1: Enable

8 Timer 7 Underflow Interrupt Enable Flag — 0: Disable 1: Enable

6 Timer 7 Compare/Capture Interrupt B Request Flag — 0: No interrupt requested 1: Interrupt requested

5 Timer 7 Compare/Capture Interrupt A Request Flag — 0: No interrupt requested 1: Interrupt requested

4 Timer 7 Underflow Interrupt Request Flag — 0: No interrupt requested 1: Interrupt requested

Set '1' when a timer 7 underflow interrupt or compare/capture interrupt occurs.

2 Timer 7 Compare/Capture Interrupt B Detect Flag — 0: No interrupt detected 1: Interrupt detected

1 Timer 7 Compare/Capture Interrupt A Detect Flag — 0: No interrupt detected 1: Interrupt detected

0 Timer 7 Underflow Interrupt Detect Flag — 0: No interrupt detected 1: Interrupt detected

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	IRQ4 TG1	IRQ4 TG0	IRQ3 TG1	IRQ3 TG0	IRQ2 TG1	IRQ2 TG0	IRQ1 TG1	IRQ1 TG0	IRQ0 TG1	IRQ0 TG0
R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

9:8 **Set Trigger Conditions for IRQ4 Pin Interrupt**
00: Low level
01: High level
10: Negative edge
11: Positive edge

7:6 **Set Trigger Conditions for IRQ3 Pin Interrupt**
00: Low level
01: High level
10: Negative edge
11: Positive edge

5:4 **Set Trigger Conditions for IRQ2 Pin Interrupt**
00: Low level
01: High level
10: Negative edge
11: Positive edge

3:2 **Set Trigger Conditions for IRQ1 Pin Interrupt**
00: Low level
01: High level
10: Negative edge
11: Positive edge

1:0 **Set Trigger Conditions for IRQ0 Pin Interrupt**
00: Low level
01: High level
10: Negative edge
11: Positive edge

EXTMD : x'00FC50'

External Interrupt Edge Setup Register

8/16-bit access register

When this is used at STOP, "L" level or "R" level should be set. At STOP, edge interrupt is not available. (Even if edge is set, interrupt occurs by level.)

E

G

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WE SHT	-	-	-	-	-	-	NALE EN	-	-	BRPG 1	BRPG 0	-	-	BREN 1	BREN 0
R/W	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R	R	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0	0	0	0	0	0	0/1	0	0	0/1	0/1	0	0	0/1	0/1

EXMCTR : x'00FD00'

External Memory Control Register

8/16-bit access register

15 **WEH, WEL Pulse Width Shortening** — 0: Disbale 1: Enable

8 **ALE Signal Polarity** — 0: Positive logic
1: Negative logic

No wait cycle in handshake mode is forbidden (address/ data separate mode) — 0: Disbale
1: Enable

Setting a page size of ROM burst mode is invalid when ROM burst mode is disabled.

5:4 **Page Size of ROM Burst Mode** — 00: 4 bytes
01: 8 bytes
10: 16 bytes
11: Reserved

1:0 **ROM Burst Mode** — 00: Disable
01: Reserved
10: Enable (without penalty)
11: Enable (with penalty)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATC EN	OVR EF	-	ATC DIR	-	-	ATC END9	ATC END8	ATC END7	ATC END6	ATC END5	ATC END4	ATC END3	ATC END2	ATC END1	ATC END0
R/W	R/W	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0/1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

ATCCTR : x'00FD10'

ATC Control Register

8/16-bit access register

15 **ATC Enable** — 0: Disbale 1: Enable

14 **Overrun Error Flag** — 0: No error 1: Error

13 **ATC Transfer Direction** — 0: From serial ch 0 to Internal RAM
1: From Internal RAm to serial ch 0

9:0 **ATC End Address** — Set the ATC end address
(the lower 10 bits of the internal RAM area)

The upper 14 bits are fixed at '00000000100000' because the internal RAM addresses for TC operation are x'008000' to x'0083FF'. Set the larger value than the ATCBC value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	ATC BC9	ATC BC8	ATC BC7	ATC BC6	ATC BC5	ATC BC4	ATC BC3	ATC BC2	ATC BC1	ATC BC0
R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

ATCBC : x'00FD12'

ATC Binary Counter

8/16-bit access register

9:0 ATC Transfer Address Set the ATC start address (the lower 10 bits of the internal RAM area) (Read the internal RAm address where the chip accesses next during ATC operation.)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC0 TEN	SC0 REN	SC0 BRE	SC0 I2CS	SC0 PTL	-	SC0 OD	SC0 I2CM	SC0 LN	SC0 PTY2	SC0 PTY1	SC0 PTY0	SC0 SB	SC0 POD	SC0 S1	SC0 S0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SC0CTR : x'00FD80'

Serial 0 Control Register

8/16-bit access register

15 Transmit Enable — 0: Disable 1: Enable

14 Receive Enable — 0: Disable 1: Enable

13 Break Transmission — 0: Don't break 1: Break (Set SBO to 0)

12 I²C Start or Stop Sequence
0: Stop sequence output when changing this bit from 1 to 0.
1: Start sequence output when changing this bit from 0 to 1.

11 Protocol Selection
0: Asynchronous mode
1: Clock synchronous mode, I²C mode

9 Bit Order Selection
0: LSB first
1: MSB first (select only when the character length is 8-bit.)

When 7-bit transfer is selected, the bit order is set only to 'LSB first'.

8 I²C mode Selection — 0: I²C mode off 1: I²C mode on

7 Character Length — 0: 7-bit 1: 8-bit

6:4 Parity Bit Selection
000: None
100: 0 (output low)
101: 1 (output high)
110: Even (1s are even)
111: Odd (1s are odd)
Others: Reserved

3 Stop Bit Selection — 0: 1-bit 1: 2-bit

The stop bit is set only during asynchronous mode.

2 Open-drain Control for I²C pin — 0: Off 1: On

1:0 Serial 0 Clock Source Selection
00: SBT0 pin
01: Timer 2 underflow/16
10: Timer 2 underflow/2
11: Timer 3 underflow/16

7	6	5	4	3	2	1	0
SC0 TRB7	SC0 TRB6	SC0 TRB5	SC0 TRB4	SC0 TRB3	SC0 TRB2	SC0 TRB1	SC0 TRB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Serial Transmit/Receive Data

SC0TRB : x'00FD82'

Serial 0 Transmit/ Receive Buffer

8-bit access register

Transmission starts by writing the data into this register. The transmission starts after 1 cycle or 2 cycles of the transmission clock. In 7-bit transfer, the MSB (bit 7) is ignored. Writing to SC0TRB register must be operated after verifying that the transmission is not in progress.

The data is received by reading this register. The data is read when an interrupt occurs or the SC0RXA flag of the SC0STR register is 1. In 7-bit transfer, the MSB (bit 7) becomes 0.

S

7	6	5	4	3	2	1	0
SC0 TBSY	SC0 RBSY	SC0 SPS	SC0 RXA	SC0 STS	SC0 FE	SC0 PE	SC0 OE
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SC0STR : x'00FD83'

Serial 0 Status Register

8-bit access register
(16-bit access is possible from even address)

7 **Transmission Busy Flag**
0: Ready to transmit
1: Transmission in progress

6 **Reception Busy Flag**
0: Ready to receive
1: Reception in progress

5 **I²C Stop Sequence Detect**
0: Undetected
1: Detected

4 **Received Data**
0: No received data
1: Received data

3 **I²C Start Sequence Detect**
0: Undetected
1: Detected

2 **Framing Error**
0: No error
1: Error

A framing error occurs when the stop bit is 0. Framing error data is updated whenever the stop bit is received.

1 **Parity Error**
0: No error
1: Error

A parity error occurs when the parity bit is 1 although it is set to 0, when the parity bit is 0 although it is set to 1, when the parity bit is odd although it is set to even, and when the parity bit is even although it is set to odd. Parity error data is updated whenever the parity bit is received.

0 **Overrun Error**
0: No error
1: Error

An overrun error occurs when the next data is received completely before the CPU reads the received data (SC0TRB). Overrun error data is updated whenever the last data bit (seventh or eighth bit) is received.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC1 TEN	SC1 REN	SC1 BRE	SC1 I2CS	SC1 PTL	-	SC1 OD	SC1 I2CM	SC1 LN	SC1 PTY2	SC1 PTY1	SC1 PTY0	SC1 SB	SC1 POD	SC1 S1	SC1 S0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SC1CTR : x'00FD90'

Serial 1 Control Register

8/16-bit access register

15 Transmit Enable 0: Disable 1: Enable

14 Receive Enable 0: Disable 1: Enable

13 Break Transmission 0: Don't break 1: Break (Set SBO to 0)

12 I²C Start or Stop Sequence
0: Stop sequence output when changing this bit from 1 to 0.
1: Start sequence output when changing this bit from 0 to 1.

11 Protocol Selection
0: Asynchronous mode
1: Clock synchronous mode, I²C mode

9 Bit Order Selection
0: LSB first
1: MSB first (select only when the character length is 8-bit.)

When 7-bit transfer is selected, the bit order is set only to 'LSB first'.

8 I²C mode Selection 0: I²C mode off 1: I²C mode on

7 Character Length 0: 7-bit 1: 8-bit

6:4 Parity Bit Selection
000: None
100: 0 (output low)
101: 1 (output high)
110: Even (1s are even)
111: Odd (1s are odd)
Others: Reserved

3 Stop Bit Selection 0: 1-bit 1: 2-bit

The stop bit is set only during asynchronous mode.

2 Open-drain Control for I²C pin 0: Off 1: On

1:0 Serial 1 Clock Source Selection
00: SBT1 pin
01: Timer 2 underflow/16
10: Timer 2 underflow/2
11: Timer 3 underflow/16

S

7	6	5	4	3	2	1	0
SC1 TRB7	SC1 TRB6	SC1 TRB5	SC1 TRB4	SC1 TRB3	SC1 TRB2	SC1 TRB1	SC1 TRB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Serial Transmit/Receive Data

SC1TRB : x'00FD92'

Serial 1 Transmit/ Receive Buffer

8-bit access register

Transmission starts by writing the data into this register. The transmission starts after 1 cycle or 2 cycles of the transmission clock. In 7-bit transfer, the MSB (bit 7) is ignored. Writing to SC1TRB register must be operated after verifying that the transmission is not in progress.

The data is received by reading this register. The data is read when an interrupt occurs or the SC1RXA flag of the SC1STR register is 1. In 7-bit transfer, the MSB (bit 7) becomes 0.

7	6	5	4	3	2	1	0
SC1 TBSY	SC1 RBSY	SC1 SPS	SC1 RXA	SC1 STS	SC1 FE	SC1 PE	SC1 OE
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SC1STR : x'00FD93'

Serial 1 Status Register

8-bit access register
(16-bit access is possible from even address)

7 **Transmission Busy Flag**
0: Ready to transmit
1: Transmission in progress

6 **Reception Busy Flag**
0: Ready to receive
1: Reception in progress

5 **I²C Stop Sequence Detect**
0: Undetected
1: Detected

4 **Received Data**
0: No received data
1: Received data

3 **I²C Start Sequence Detect**
0: Undetected
1: Detected

2 **Framing Error**
0: No error
1: Error

A framing error occurs when the stop bit is 0. Framing error data is updated whenever the stop bit is received.

1 **Parity Error**
0: No error
1: Error

A parity error occurs when the parity bit is 1 although it is set to 0, when the parity bit is 0 although it is set to 1, when the parity bit is odd although it is set to even, and when the parity bit is even although it is set to odd. Parity error data is updated whenever the parity bit is received.

0 **Overrun Error**
0: No error
1: Error

An overrun error occurs when the next data is received completely before the CPU reads the received data (SC1TRB). Overrun error data is updated whenever the last data bit (seventh or eighth bit) is received.

S

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	AN NCH2	AN NCH1	AN NCH0	-	AN 1CH2	AN 1CH1	AN 1CH0	AN EN	AN TM1	-	-	AN CK1	AN CK0	AN MD1	AN MD0
R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	0/1	0	0	0/1	0/1	0/1	0/1

ANCTR : x'00FDA0'

A/D Converter Control Register

8/16-bit access register

14:12 Channel Selection for Multiple Channel Conversion

000: Convert AN0
001: Convert from AN0 to AN1
010: Convert from AN0 to AN2
011: Convert from AN0 to AN3
100: Convert from AN0 to AN4
101: Convert from AN0 to AN5
110: Convert from AN0 to AN6
111: Convert from AN0 to AN7

10:8 Channel Selection for Single Channel Conversion

000: Convert AN0
001: Convert AN1
010: Convert AN2
011: Convert AN3
100: Convert AN4
101: Convert AN5
110: Convert AN6
111: Convert AN7

7 Conversion Start/Execution Flag

0: Reserved
1: Conversion start/Conversion in progress

6 Conversion Start at Timer 1 underflow

0: Disable
1: Enable

3:2 Clock Source Selection

00: SYSCLK
01: SYSCLK/2
10: SYSCLK/4
11: SYSCLK/8

At 1.0 MHz to 20 MHz oscillation, b'10' and b'11' are available. At 5 MHz to 10 MHz oscillation, b'01', b'10' and b'11' are available. At under 5 MHz oscillation, all of these are available.

1:0 Operating Mode Selection

00: Single channel, single conversion
01: Multiple channels, single conversion
10: Single channel, continuous conversion
11: Multiple channels, continuous conversion

7	6	5	4	3	2	1	0
AN0 BUF7	AN0 BUF6	AN0 BUF5	AN0 BUF4	AN0 BUF3	AN0 BUF2	AN0 BUF1	AN0 BUF0
R	R	R	R	R	R	R	R
*Note	*Note	*Note	*Note	*Note	*Note	*Note	*Note
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Undefined

7:0 A/D Conversion Result of Ch 0 (AN0 Pin)

AN0BUF : x'00FDA8'

A/D 0 Conversion Data Buffer

8/16-bit access register

AN0BUF is a read-only buffer.

7	6	5	4	3	2	1	0
AN1 BUF7	AN1 BUF6	AN1 BUF5	AN1 BUF4	AN1 BUF3	AN1 BUF2	AN1 BUF1	AN1 BUF0
R	R	R	R	R	R	R	R
*Note	*Note	*Note	*Note	*Note	*Note	*Note	*Note
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Undefined

7:0 A/D Conversion Result of Ch 1 (AN1 Pin)

AN1BUF : x'00FDA9'

A/D 1 Conversion Data Buffer

8-bit access register
(16-bit access is possible from even address)

AN1BUF is a read-only buffer.

7	6	5	4	3	2	1	0
AN2 BUF7	AN2 BUF6	AN2 BUF5	AN2 BUF4	AN2 BUF3	AN2 BUF2	AN2 BUF1	AN2 BUF0
R	R	R	R	R	R	R	R
*Note	*Note	*Note	*Note	*Note	*Note	*Note	*Note
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Undefined

7:0 A/D Conversion Result of Ch 2 (AN2 Pin)

AN2BUF : x'00FDAA'

A/D 2 Conversion Data Buffer

8/16-bit access register

AN2BUF is a read-only buffer.

7	6	5	4	3	2	1	0
AN3 BUF7	AN3 BUF6	AN3 BUF5	AN3 BUF4	AN3 BUF3	AN3 BUF2	AN3 BUF1	AN3 BUF0
R	R	R	R	R	R	R	R
*Note	*Note	*Note	*Note	*Note	*Note	*Note	*Note
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Undefined

7:0 A/D Conversion Result of Ch 3 (AN3 Pin)

AN3BUF : x'00FDAB'

A/D 3 Conversion Data Buffer

8-bit access register (16-bit access is possible from even address)

AN3BUF is a read-only buffer.

7	6	5	4	3	2	1	0
AN4 BUF7	AN4 BUF6	AN4 BUF5	AN4 BUF4	AN4 BUF3	AN4 BUF2	AN4 BUF1	AN4 BUF0
R	R	R	R	R	R	R	R
*Note	*Note	*Note	*Note	*Note	*Note	*Note	*Note
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Undefined

7:0 A/D Conversion Result of Ch 4 (AN4 Pin)

AN4BUF : x'00FDAC'

A/D 4 Conversion Data Buffer

8/16-bit access register

AN4BUF is a read-only buffer.

7	6	5	4	3	2	1	0
AN5 BUF7	AN5 BUF6	AN5 BUF5	AN5 BUF4	AN5 BUF3	AN5 BUF2	AN5 BUF1	AN5 BUF0
R	R	R	R	R	R	R	R
*Note	*Note	*Note	*Note	*Note	*Note	*Note	*Note
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Undefined

7:0 A/D Conversion Result of Ch 5 (AN5 Pin)

AN5BUF : x'00FDAD'

A/D 5 Conversion Data Buffer

8-bit access register (16-bit access is possible from even address)

AN5BUF is a read-only buffer.

7	6	5	4	3	2	1	0
AN6 BUF7	AN6 BUF6	AN6 BUF5	AN6 BUF4	AN6 BUF3	AN6 BUF2	AN6 BUF1	AN6 BUF0
R	R	R	R	R	R	R	R
*Note	*Note	*Note	*Note	*Note	*Note	*Note	*Note
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Undefined

7:0 A/D Conversion Result of Ch 6 (AN6 Pin)

AN6BUF : x'00FDAE'

A/D 6 Conversion Data Buffer

8/16-bit access register

AN6BUF is a read-only buffer.

7	6	5	4	3	2	1	0
AN7 BUF7	AN7 BUF6	AN7 BUF5	AN7 BUF4	AN7 BUF3	AN7 BUF2	AN7 BUF1	AN7 BUF0
R	R	R	R	R	R	R	R
*Note	*Note	*Note	*Note	*Note	*Note	*Note	*Note
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Undefined

7:0 A/D Conversion Result of Ch 7 (AN7 Pin)

AN7BUF : x'00FDAF'

A/D 7 Conversion Data Buffer

8-bit access register
(16-bit access is possible from even address)

AN7BUF is a read-only buffer.

7	6	5	4	3	2	1	0
TM0 BC7	TM0 BC6	TM0 BC5	TM0 BC4	TM0 BC3	TM0 BC2	TM0 BC1	TM0 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 0 Count Value

TM0BC : x'00FE00'

Timer 0 Binary Counter

8/16-bit access register

TM0BC is a read-only register.

7	6	5	4	3	2	1	0
TM1 BC7	TM1 BC6	TM1 BC5	TM1 BC4	TM1 BC3	TM1 BC2	TM1 BC1	TM1 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 1 Count Value

TM1BC : x'00FE01'

Timer 1 Binary Counter

8-bit access register
(16-bit access is possible from even address)

TM1BC is a read-only register.

7	6	5	4	3	2	1	0
TM2 BC7	TM2 BC6	TM2 BC5	TM2 BC4	TM2 BC3	TM2 BC2	TM2 BC1	TM2 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 2 Count Value

TM2BC : x'00FE02'

Timer 2 Binary Counter

8/16-bit access register

TM2BC is a read-only register.

7	6	5	4	3	2	1	0
TM3 BC7	TM3 BC6	TM3 BC5	TM3 BC4	TM3 BC3	TM3 BC2	TM3 BC1	TM3 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 3 Count Value

TM3BC : x'00FE03'

Timer 3 Binary Counter

8-bit access register (16-bit access is possible from even address)

TM3BC is a read-only register.

7	6	5	4	3	2	1	0
TM4 BC7	TM4 BC6	TM4 BC5	TM4 BC4	TM4 BC3	TM4 BC2	TM4 BC1	TM4 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 4 Count Value

TM4BC : x'00FE04'

Timer 4 Binary Counter

8/16-bit access register

TM4BC is a read-only register.

7	6	5	4	3	2	1	0
TM5 BC7	TM5 BC6	TM5 BC5	TM5 BC4	TM5 BC3	TM5 BC2	TM5 BC1	TM5 BC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Timer 5 Count Value

TM5BC : x'00FE05'

Timer 5 Binary Counter

8-bit access register (16-bit access is possible from even address)

TM5BC is a read-only register.

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7	6	5	4	3	2	1	0
TM0 BR7	TM0 BR6	TM0 BR5	TM0 BR4	TM0 BR3	TM0 BR2	TM0 BR1	TM0 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM0BR : x'00FE10'

Timer 0 Base Register

8/16-bit access register

7:0 Timer 0 Count Cycle

Set the count cycle (2 to 256). Timer 0 counts the set value plus 1. The valid range for TM0BR is 0 to 255.

TM0BR is set to 0 after timer 0 starts. See "4-2 8-bit Timer Setup Examples" for details.

7	6	5	4	3	2	1	0
TM1 BR7	TM1 BR6	TM1 BR5	TM1 BR4	TM1 BR3	TM1 BR2	TM1 BR1	TM1 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM1BR : x'00FE11'

Timer 1 Base Register

8-bit access register (16-bit access is possible from even address)

7:0 Timer 1 Count Cycle

Set the count cycle (2 to 256). Timer 1 counts the set value plus 1. The valid range for TM1BR is 0 to 255.

TM1BR is set to 0 after timer 1 starts. See "4-2 8-bit Timer Setup Examples" for details.

7	6	5	4	3	2	1	0
TM2 BR7	TM2 BR6	TM2 BR5	TM2 BR4	TM2 BR3	TM2 BR2	TM2 BR1	TM2 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM2BR : x'00FE12'

Timer 2 Base Register

8/16-bit access register

7:0 Timer 2 Count Cycle

Set the count cycle (2 to 256). Timer 2 counts the set value plus 1. The valid range for TM2BR is 0 to 255.

TM2BR is set to 0 after timer 2 starts. See "4-2 8-bit Timer Setup Examples" for details.

7	6	5	4	3	2	1	0
TM3 BR7	TM3 BR6	TM3 BR5	TM3 BR4	TM3 BR3	TM3 BR2	TM3 BR1	TM3 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM3BR : x'00FE13'

Timer 3 Base Register

8-bit access register (16-bit access is possible from even address)

TM3BR is set to 0 after timer 3 starts. See "4-2 8-bit Timer Setup Examples" for details.

7:0 Timer 3 Count Cycle

Set the count cycle (2 to 256). Timer 3 counts the set value plus 1. The valid range for TM3BR is 0 to 255.

7	6	5	4	3	2	1	0
TM4 BR7	TM4 BR6	TM4 BR5	TM4 BR4	TM4 BR3	TM4 BR2	TM4 BR1	TM4 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM4BR : x'00FE14'

Timer 4 Base Register

8/16-bit access register

TM4BR is set to 0 after timer 4 starts. See "4-2 8-bit Timer Setup Examples" for details.

7:0 Timer 4 Count Cycle

Set the count cycle (2 to 256). Timer 4 counts the set value plus 1. The valid range for TM4BR is 0 to 255.

7	6	5	4	3	2	1	0
TM5 BR7	TM5 BR6	TM5 BR5	TM5 BR4	TM5 BR3	TM5 BR2	TM5 BR1	TM5 BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM5BR : x'00FE15'

Timer 5 Base Register

8-bit access register (16-bit access is possible from even address)

TM5BR is set to 0 after timer 5 starts. See "4-2 8-bit Timer Setup Examples" for details.

7:0 Timer 5 Count Cycle

Set the count cycle (2 to 256). Timer 5 counts the set value plus 1. The valid range for TM4BR is 0 to 255.

T

7	6	5	4	3	2	1	0
TM0 EN	TM0 LD	-	-	-	-	TM0 S1	TM0 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

TM0MD : x'00FE20'

Timer 0 Mode Register

8/16-bit access register

7 TM0BC Count
0: Disable
1: Enable

6 TM0BR Setup
0: Disable
1: Load TM0BR to TM0BC,
Reset the 1/2 divisor circuit,
Fix TMIO output to 0.

1:0 Clock Source Selection
00: TM0IO pin clock (Event timer)
01: System clock/128
10: System clock
11: Low-speed clock (32 kHz)/4

7	6	5	4	3	2	1	0
TM1 EN	TM1 LD	-	-	-	-	TM1 S1	TM1 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

TM1MD : x'00FE21'

Timer 1 Mode Register

8-bit access register
(16-bit access is possible from even address)

7 TM1BC Count
0: Disable
1: Enable

6 TM1BR Setup
0: Disable
1: Load TM1BR to TM1BC,
Reset the 1/2 divisor circuit,
Fix TMIO output to 0.

1:0 Clock Source Selection
00: TM1IO pin clock (Event timer)
01: Low-speed clock (32 kHz)/4
10: Timer 0 output clock
11: System clock

7	6	5	4	3	2	1	0
TM2 EN	TM2 LD	-	-	-	-	TM2 S1	TM2 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

TM2MD : x'00FE22'

Timer 2 Mode Register

8/16-bit access register

7 TM2BC Count
0: Disable
1: Enable

6 TM2BR Setup
0: Disable
1: Load TM2BR to TM2BC,
Reset the 1/2 divisor circuit,
Fix TMIO output to 0.

1:0 Clock Source Selection
00: TM2IO pin clock (Event timer)
01: Timer 1 cascade
10: Timer 0 output clock
11: System clock

7	6	5	4	3	2	1	0
TM3 EN	TM3 LD	-	-	-	-	TM3 S1	TM3 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

TM3MD : x'00FE23'

Timer 3 Mode Register

8-bit access register
(16-bit access is possible from even address)

7 TM3BC Count
0: Disable
1: Enable

6 TM3BR Setup
0: Disable
1: Load TM3BR to TM3BC,
Reset the 1/2 divisor circuit,
Fix TMIO output to 0.

1:0 Clock Source Selection
00: TM3IO pin clock (Event timer)
01: Timer 2 cascade
10: Timer 0 output clock
11: System clock

T

7	6	5	4	3	2	1	0
TM4 EN	TM4 LD	-	-	-	-	TM4 S1	TM4 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

TM4MD : x'00FE24'

Timer 4 Mode Register

8/16-bit access register

7 TM4BC Count
0: Disable
1: Enable

6 TM4BR Setup
0: Disable
1: Load TM4BR to TM4BC,
Reset the 1/2 divisor circuit,
Fix TMIO output to 0.

1:0 Clock Source Selection
00: TM4IO pin clock (Event timer)
01: Timer 3 cascade
10: Timer 0 output clock
11: Low-speed clock (32 kHz)/4

7	6	5	4	3	2	1	0
TM5 EN	TM5 LD	-	-	-	-	TM5 S1	TM5 S0
R/W	R/W	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0	0	0/1	0/1

TM5MD : x'00FE25'

Timer 5 Mode Register

8-bit access register
(16-bit access is possible from even address)

7 TM5BC Count
0: Disable
1: Enable

6 TM5BR Setup
0: Disable
1: Load TM5BR to TM5BC,
Reset the 1/2 divisor circuit,
Fix TMIO output to 0.

1:0 Clock Source Selection
00: TM5IO pin clock (Event timer)
01: Timer 4 cascade
10: Timer 0 output clock
11: Low-speed clock (32 kHz)/4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 EN	TM6 NLD	-	-	TM6 UD1	TM6 UD0	TM6 TGE	TM6 ONE	TM6 MD1	TM6 MD0	TM6 ECLR	TM6 LP	TM6 ASEL	TM6 S2	TM6 S1	TM6 S0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM6MD : x'00FE30'

Timer 6 Mode Register

16-bit access register

15 TM6BC Count 0: Disable 1: Enable

14 TM6BC, T.F.F., RS.F.F. Operation
0: Set TM6BC, T.F.F., RS.F.F. to 0
1: Operate TM6BC, T.F.F., RS.F.F.

11:10 Up/Down Counter Mode Selection (Ignored when two-phase encoding is selected.)
00: Up counter
01: Down counter
10: Up when TM6IOA pin is high, down when TM6IOA pin is low
11: Up when TM6IOB pin is high, down when TM6IOB pin is low

Selecting up/down counting mode is ignored when two-phase encoding is slected.

9 Count Start External Trigger Enable 0: Disable 1: Enable

Counting starts on the falling edge of TM6IOB pin.
Clear TM6EN when TM6BC matches TM6CA.

8 Counter Operating Mode Select 0: Repeat 1: One-shot counting

During repeat counting, hold the TM6EN flag state. During one-shot counting, set the TM6EN flag to 0 when TM6BC=TM6CA.

7:6 TM6CA, TM6CB Operating Mode Selection
00: Compare register (single buffer)
01: Compare register (double buffer)
10: Capture A when TM6IOA pin is high, Capture B when TM6IOA pin is low
11: Capture A when TM6IOA pin is high, Capture B when TM6IOB pin is high

5 TM6BC Clear When TM6IC is 1 0: Don't clear 1: Clear*

* Clear TM6BC synchronizing externally.

4 TM6BC Clear/TM6CA Reload
When TM6BC=TM6CA while up counting
0: Don't clear TM6BC 1: Clear TM6BC**
When TM6BC=0 while down counting
0: Don't reload TM6CA 1: Reload TM6CA***

** Clear TM6BC when PWM is output.

*** When TM6LP is 1 and up-counting is selected, TM6BC is cleared to 0 on the next cycle if TM6BC counts until TM6BC matches TM6CA or x'FFFF'. When down counting is selected, TM6BC is set to TM6CA on the next cycle regardless of this bit setting if TM6BC becomes 0.

3 TM6IOA Pin Output
0: RS.F.F. output (one-phase PWM)
1: T.F.F. output (two-phase PWM)

2:0 Clock Source Selection
000: Timer 4 output
001: Timer 5 output
010: TM6IOB pin clock
011: SYSCLK
100: Two-phase encoder (4x) of TM6IOA pin, TM6IOB pin
101: Two-phase encoder (1x) of TM6IOA pin, TM6IOB pin
11*: Reserved

T

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 BC15	TM6 BC14	TM6 BC13	TM6 BC12	TM6 BC11	TM6 BC10	TM6 BC9	TM6 BC8	TM6 BC7	TM6 BC6	TM6 BC5	TM6 BC4	TM6 BC3	TM6 BC2	TM6 BC1	TM6 BC0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM6BC : x'00FE32'

Timer 6 Binary Counter

16-bit access register

TM6BC is a read-only register.

15:0 Timer 6 Count Value

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CA15	TM6 CA14	TM6 CA13	TM6 CA12	TM6 CA11	TM6 CA10	TM6 CA9	TM6 CA8	TM6 CA7	TM6 CA6	TM6 CA5	TM6 CA4	TM6 CA3	TM6 CA2	TM6 CA1	TM6 CA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM6CA : x'00FE34'

Timer 6 Compare/ Capture Register A

16-bit access register

When capture is selected, TM6CA reads the captured values and a timer 6 capture A interrupt is generated when capture occurs. When compare is selected, set the PWM cycle. When this register matches the timer 6 binary counter, a timer 6 capture A interrupt occurs.

15:0 Timer 6 Count Cycle Set the count cycle minus 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM6 CB15	TM6 CB14	TM6 CB13	TM6 CB12	TM6 CB11	TM6 CB10	TM6 CB9	TM6 CB8	TM6 CB7	TM6 CB6	TM6 CB5	TM6 CB4	TM6 CB3	TM6 CB2	TM6 CB1	TM6 CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM6CB : x'00FE38'

Timer 6 Compare/ Capture Register B

16-bit access register

When capture is selected, TM6CB reads the captured values and a timer 6 capture B interrupt is generated when capture occurs. When compare is selected, set the PWM cycle. When this register matches the timer 6 binary counter, a timer 6 capture B interrupt occurs.

15:0 Timer 6 PWM Change or Interrupt Generation

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 EN	TM7 NLD	-	-	TM7 UD1	TM7 UD0	TM7 TGE	TM7 ONE	TM7 MD1	TM7 MD0	TM7 ECLR	TM7 LP	TM7 ASEL	TM7 S2	TM7 S1	TM7 S0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM7MD : x'00FE40'

Timer 7 Mode Register

16-bit access register

15 TM7BC Count 0: Disable 1: Enable

14 TM7BC, T.F.F., RS.F.F. Operation
0: Set TM7BC, T.F.F., RS.F.F. to 0
1: Operate TM7BC, T.F.F., RS.F.F.

11:10 Up/Down Counter Mode Selection (Ignored when two-phase encoding is selected.)
00: Up counter
01: Down counter
10: Up when TM7IOA pin is high, down when TM7IOA pin is low
11: Up when TM7IOB pin is high, down when TM7IOB pin is low

Selecting up/down counting mode is ignored when two-phase encoding is slected.

9 Count Start External Trigger Enable 0: Disable 1: Enable

Counting starts on the falling edge of TM7IOB pin.
Clear TM7EN when TM7BC matches TM7CA.

8 Counter Operating Mode Select 0: Repeat 1: One-shot counting

During repeat counting, hold the TM7EN flag state. During one-shot counting, set the TM7EN flag to 0 when TM7BC=TM7CA.

7:6 TM7CA, TM7CB Operating Mode Selection
00: Compare register (single buffer)
01: Compare register (double buffer)
10: Capture A when TM7IOA pin is high, Capture B when TM7IOA pin is low
11: Capture A when TM7IOA pin is high, Capture B when TM7IOB pin is high

5 TM7BC Clear When TM6IC is 1 0: Don't clear 1: Clear*

* Clear TM7BC synchronizing externally.

4 TM7BC Clear/TM7CA Reload
When TM7BC=TM7CA while up counting
0: Don't clear TM7BC 1: Clear TM7BC**
When TM7BC=0 while down counting
0: Don't reload TM7CA 1: ReloadTM7CA***

** Clear TM7BC when PWM is output.

*** When TM7LP is 1 and up-counting is selected, TM7BC is cleared to 0 on the next cycle if TM7BC counts until TM7BC matches TM7CA or x'FFFF'. When down counting is selected, TM7BC is set to TM7CA on the next cycle regardless of this bit setting if TM7BC becomes 0.

3 TM7IOA Pin Output
0: RS.F.F. output (one-phase PWM)
1: T.F.F. output (two-phase PWM)

2:0 Clock Source Selection
000: Timer 4 output
001: Timer 5 output
010: TM7IOB pin clock
011: SYSCLK
100: Two-phase encoder (4x) of TM7IOA pin, TM7IOB pin
101: Two-phase encoder (1x) of TM7IOA pin, TM7IOB pin
11*: Reserved

T

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 BC15	TM7 BC14	TM7 BC13	TM7 BC12	TM7 BC11	TM7 BC10	TM7 BC9	TM7 BC8	TM7 BC7	TM7 BC6	TM7 BC5	TM7 BC4	TM7 BC3	TM7 BC2	TM7 BC1	TM7 BC0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM7BC : x'00FE42'

Timer 7 Binary Counter

16-bit access register

TM7BC is a read-only register.

15:0 Timer 7 Count Value

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CA15	TM7 CA14	TM7 CA13	TM7 CA12	TM7 CA11	TM7 CA10	TM7 CA9	TM7 CA8	TM7 CA7	TM7 CA6	TM7 CA5	TM7 CA4	TM7 CA3	TM7 CA2	TM7 CA1	TM7 CA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM7CA : x'00FE44'

Timer 7 Compare/ Capture Register A

16-bit access register

When capture is selected, TM7CA reads the captured values and a timer 7 capture A interrupt is generated when capture occurs. When compare is selected, set the PWM cycle. When this register matches the timer 7 binary counter, a timer 7 capture A interrupt occurs.

15:0 Timer 7 Count Cycle Set the count cycle minus 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM7 CB15	TM7 CB14	TM7 CB13	TM7 CB12	TM7 CB11	TM7 CB10	TM7 CB9	TM7 CB8	TM7 CB7	TM7 CB6	TM7 CB5	TM7 CB4	TM7 CB3	TM7 CB2	TM7 CB1	TM7 CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TM7CB : x'00FE48'

Timer 7 Compare/ Capture Register B

16-bit access register

When capture is selected, TM7CB reads the captured values and a timer 7 capture B interrupt is generated when capture occurs. When compare is selected, set the PWM cycle. When this register matches the timer 7 binary counter, a timer 7 capture B interrupt occurs.

15:0 Timer 7 PWM Change or Interrupt Generation

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WBSWP 15	WBSWP 14	WBSWP 13	WBSWP 12	WBSWP 11	WBSWP 10	WBSWP 9	WBSWP 8	WBSWP 7	WBSWP 6	WBSWP 5	WBSWP 4	WBSWP 3	WBSWP 2	WBSWP 1	WBSWP 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WBSWP 7	WBSWP 6	WBSWP 5	WBSWP 4	WBSWP 3	WBSWP 2	WBSWP 1	WBSWP 0	WBSWP 15	WBSWP 14	WBSWP 13	WBSWP 12	WBSWP 11	WBSWP-10	WBSWP 9	WBSWP 8

WBSWP : x'00FFA0'

Word Data Byte Swap Register

8/16-bit access register

15:0 Word Data Byte Swap Data — During read operations, the upper 8 bits and the lower 8 bits are swapped.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBSWP 15	PBSWP 14	PBSWP 13	PBSWP 12	PBSWP 11	PBSWP 10	PBSWP 9	PBSWP 8	PBSWP 7	PBSWP 6	PBSWP 5	PBSWP 4	PBSWP 3	PBSWP 2	PBSWP 1	PBSWP 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PBSWP 15	PBSWP 14	PBSWP 13	PBSWP 12	PBSWP 11	PBSWP 10	PBSWP 9	PBSWP 8	PBSWP 23	PBSWP 22	PBSWP 21	PBSWP 20	PBSWP 19	PBSWP 18	PBSWP 17	PBSWP 16

PBSWPL : x'00FFA2'

Pointer Data Byte Swap Register (Lower)

8/16-bit access register

15:0 Pointer Data Byte Swap Data — During read operations, the upper 8 bits are remain and the lower 8 bits of PBSWPH are read out in the lower 8 bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	PBSWP 23	PBSWP 22	PBSWP 21	PBSWP 20	PBSWP 19	PBSWP 18	PBSWP 17	PBSWP 16
-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	PBSWP 7	PBSWP 6	PBSWP 5	PBSWP 4	PBSWP 3	PBSWP 2	PBSWP 1	PBSWP 0

PBSWPH : x'00FFA4'

Pointer Data Byte Swap Register (Upper)

8/16-bit access register

7:0 Pointer Data Byte Swap Data — During read operations, the lower 8 bits of PBSWPL are read out in the upper 8 bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBSWP 15	LBSWP 14	LBSWP 13	LBSWP 12	LBSWP 11	LBSWP 10	LBSWP 9	LBSWP 8	LBSWP 7	LBSWP 6	LBSWP 5	LBSWP 4	LBSWP 3	LBSWP 2	LBSWP 1	LBSWP 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LBSWP 23	LBSWP 22	LBSWP 21	LBSWP 20	LBSWP 19	LBSWP 18	LBSWP 17	LBSWP 16	LBSWP 31	LBSWP 30	LBSWP 29	LBSWP 28	LBSWP 27	LBSWP 26	LBSWP 25	LBSWP 24

LBSWPL : x'00FFA6'

Long-word Data Byte Swap Register (Lower)

8/16-bit access register

15:0 Long-word Data Byte Swap Data — During read operations, the lower 8 bits of LBSWPH are read out in the upper 8 bits and the upper 8 bits of LBSWPH are read out in the lower 8 bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBSWP 31	LBSWP 30	LBSWP 29	LBSWP 28	LBSWP 27	LBSWP 26	LBSWP 25	LBSWP 24	LBSWP 23	LBSWP 22	LBSWP 21	LBSWP 20	LBSWP 19	LBSWP 18	LBSWP 17	LBSWP 16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LBSWP 7	LBSWP 6	LBSWP 5	LBSWP 4	LBSWP 3	LBSWP 2	LBSWP 1	LBSWP 0	LBSWP 15	LBSWP 14	LBSWP 13	LBSWP 12	LBSWP 11	LBSWP 10	LBSWP 9	LBSWP 8

LBSWPH : x'00FFA8'

Long-word Data Byte Swap Register (Upper)

8/16-bit access register

15:0 Long-word Data Byte Swap Data

During read operations, the lower 8 bits of LBSWPL are read out in the upper 8 bits and the upper 8 bits of LBSWPL are read out in the lower 8 bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*Note	SB1P	SB0P	PA4P	PA3P	PA2P	PA1P	PA0P	CSP	REWEP	P60P	AHP	AMP	ALP	DHP	DLP
R	R/W	R/W	R/w	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Always set 0.

PPLU : x'00FFB0'

Port Pullup Control Register

16-bit access register

Always set bit 15 to 0.

14 **Pullup Resistors of Serial 1 Related Pins (SBT1, SBI1, SBO1)** 0: Off 1: On

13 **Pullup Resistors of Serial 0 Related Pins (SBT0, SBI0, SBO0)** 0: Off 1: On

12 **Pullup Resistor of IRQ4 (PA4)** 0: Off 1: On

11 **Pullup Resistor of IRQ3 (PA3)** 0: Off 1: On

10 **Pullup Resistor of IRQ2 (PA2)** 0: Off 1: On

9 **Pullup Resistor of IRQ1 (PA1)** 0: Off 1: On

8 **Pullup Resistor of IRQ0 (PA0)** 0: Off 1: On

7 **Pullup Resistors of /CS3 to /CS0** 0: Off 1: On

6 **Pullup Resistors of External Memory Related Pins (/RE, /BSTRE, /WEH, /WEL)** 0: Off 1: On

5 **Pullup Resistor of WAIT (P60)** 0: Off 1: On

4 **Pullup Resistors of A23 to A16** 0: Off 1: On

3 **Pullup Resistors of A15 to A8** 0: Off 1: On

2 **Pullup Resistors of A7 to A0** 0: Off 1: On

1 **Pullup Resistors of D15 to D8** 0: Off 1: On

0 **Pullup Resistors of D7 to D0** 0: Off 1: On

7	6	5	4	3	2	1	0
P0 OUT7	P0 OUT6	P0 OUT5	P0 OUT4	P0 OUT3	P0 OUT2	P0 OUT1	P0 OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 0 Output

P0OUT : x'00FFC0'

Port 0 Output Register

8/16-bit access register

7	6	5	4	3	2	1	0
P1 OUT7	P1 OUT6	P1 OUT5	P1 OUT4	P1 OUT3	P1 OUT2	P1 OUT1	P1 OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 1 Output

P1OUT : x'00FFC1'

Port 1 Output Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
P2 OUT7	P2 OUT6	P2 OUT5	P2 OUT4	P2 OUT3	P2 OUT2	P2 OUT1	P2 OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 2 Output

P2OUT : x'00FFC2'

Port 2 Output Register

8/16-bit access register

7	6	5	4	3	2	1	0
P3 OUT7	P3 OUT6	P3 OUT5	P3 OUT4	P3 OUT3	P3 OUT2	P3 OUT1	P3 OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 3 Output

P3OUT : x'00FFC3'

Port 3 Output Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
P4 OUT7	P4 OUT6	P4 OUT5	P4 OUT4	P4 OUT3	P4 OUT2	P4 OUT1	P4 OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 4 Output

P4OUT : x'00FFC4'

Port 4 Output Register

8/16-bit access register

7	6	5	4	3	2	1	0
P5 OUT7	P5 OUT6	P5 OUT5	P5 OUT4	P5 OUT3	P5 OUT2	P5 OUT1	P5 OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 5 Output

P5OUT : x'00FFC5'

Port 5 Output Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
-	-	-	-	P6 OUT3	P6 OUT2	P6 OUT1	P6 OUT0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1

3:0 Port 6 Output

P6OUT : x'00FFC6'

Port 6 Output Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	P7 OUT5	P7 OUT4	P7 OUT3	P7 OUT2	P7 OUT1	P7 OUT0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

5:0 Port 7 Output

P7OUT : x'00FFC7'

Port 7 Output Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
P8 OUT7	P8 OUT6	P8 OUT5	P8 OUT4	P8 OUT3	P8 OUT2	P8 OUT1	P8 OUT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 8 Output

P8OUT : x'00FFC8'

Port 8 Output Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	-	-	P9 OUT3	P9 OUT2	P9 OUT1	P9 OUT0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1

3:0 Port 9 Output

P9OUT : x'00FFC9'

Port 9 Output Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
-	-	PA OUT5	PA OUT4	PA OUT3	PA OUT2	PA OUT1	PA OUT0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

5:0 Port A Output

PAOUT : x'00FFCA'

Port A Output Register

8/16-bit access register

7	6	5	4	3	2	1	0
P0 IN7	P0 IN6	P0 IN5	P0 IN4	P0 IN3	P0 IN2	P0 IN1	P0 IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 0 Input

P0IN : x'00FFD0'

Port 0 Input Register

8/16-bit access register

7	6	5	4	3	2	1	0
P1 IN7	P1 IN6	P1 IN5	P1 IN4	P1 IN3	P1 IN2	P1 IN1	P1 IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 1 Input

P1IN : x'00FFD1'

Port 1 Input Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
P2 IN7	P2 IN6	P2 IN5	P2 IN4	P2 IN3	P2 IN2	P2 IN1	P2 IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 2 Input

P2IN : x'00FFD2'

Port 2 Input Register

8/16-bit access register

7	6	5	4	3	2	1	0
P3 IN7	P3 IN6	P3 IN5	P3 IN4	P3 IN3	P3 IN2	P3 IN1	P3 IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 3 Input

P3IN : x'00FFD3'

Port 3 Input Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
P4 IN7	P4 IN6	P4 IN5	P4 IN4	P4 IN3	P4 IN2	P4 IN1	P4 IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 4 Input

P4IN : x'00FFD4'

Port 4 Input Register

8/16-bit access register

7	6	5	4	3	2	1	0
P5 IN7	P5 IN6	P5 IN5	P5 IN4	P5 IN3	P5 IN2	P5 IN1	P5 IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 5 Input

P5IN : x'00FFD5'

Port 5 Input Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
-	-	-	-	P6 IN3	P6 IN2	P6 IN1	P6 IN0
R	R	R	R	R	R	R	R
0	0	0	0	Port	Port	Port	Port
0	0	0	0	0/1	0/1	0/1	0/1

3:0 Port 6 Input

P6IN : x'00FFD6'

Port 6 Input Register

8/16-bit access register

7	6	5	4	3	2	1	0
-	-	P7 IN5	P7 IN4	P7 IN3	P7 IN2	P7 IN1	P7 IN0
R	R	R	R	R	R	R	R
1	1	Port	Port	Port	Port	Port	Port
1	1	0/1	0/1	0/1	0/1	0/1	0/1

5:0 Port 7 Input

P7IN : x'00FFD7'

Port 7 Input Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
P8 IN7	P8 IN6	P8 IN5	P8 IN4	P8 IN3	P8 IN2	P8 IN1	P8 IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 8 Input

P8IN : x'00FFD8'

Port 8 Input Register

8/16-bit access register

7	6	5	4	3	2	1	0
P9 IN7	P9 IN6	P9 IN5	P9 IN4	P9 IN3	P9 IN2	P9 IN1	P9 IN0
R	R	R	R	R	R	R	R
Port	Port	Port	Port	Port	Port	Port	Port
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Port 9 Input

P9IN : x'00FFD9'

Port 9 Input Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
-	NMI	PA IN5	PA IN4	PA IN3	PA IN2	PA IN1	PA IN0
R	R	R	R	R	R	R	R
0	NMI	Port	Port	Port	Port	Port	Port
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

5:0 Port A Input

PAIN : x'00FFDA'

Port A Input Register

8-bit access register
(16-bit access is possible from even address)

Bit 6 is the level of /NMI pin.

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P0 DIR0
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0/1

0 All Pin Input/Output of Port 0 0: Input
1: Output

P0DIR : x'00FFE0'

Port 0 Input/Output Control Register

8/16-bit access register

Setting 1 is allowed only when port 0 is used.

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P1 DIR0
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0/1

0 All Pin Input/Output of Port 1 0: Input
1: Output

P1DIR : x'00FFE1'

Port 1 Input/Output Control Register

8-bit access register
(16-bit access is possible from even address)

Setting 1 is allowed only when port 1 is used.

7	6	5	4	3	2	1	0
-	-	-	P2 DIR4	-	-	-	P2 DIR0
R	R	R	R/W	R	R	R	R/W
0	0	0	0	0	0	0	0
0	0	0	0/1	0	0	0	0/1

4 **Bits [7:4] Input/Output of Port 2** 0: Input
1: Output

0 **Bits [3:0] Input/Output of Port 2** 0: Input
1: Output

P2DIR : x'00FFE2'

Port 2 Input/Output Control Register

8/16-bit access register

Selecting 1 is not allowed in address/data separated mode during processor mode.

7	6	5	4	3	2	1	0
P3 DIR7	P3 DIR6	P3 DIR5	P3 DIR4	P3 DIR3	P3 DIR2	P3 DIR1	P3 DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 **Each Pin Input/Output of Port 3** 0: Input
1: Output

P3DIR : x'00FFE3'

Port 3 Input/Output Control Register

8-bit access register
(16-bit access is possible from even address)

Selecting 1 is not allowed in address/data separated mode during processor mode.

P

7	6	5	4	3	2	1	0
P4 DIR7	P4 DIR6	P4 DIR5	P4 DIR4	P4 DIR3	P4 DIR2	P4 DIR1	P4 DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 **Each Pin Input/Output of Port 4** 0: Input
1: Output

P4DIR : x'00FFE4'

Port 4 Input/Output Control Register

8/16-bit access register

Selecting 1 is not allowed in address/data separated mode during processor mode.

7	6	5	4	3	2	1	0
P5 DIR7	P5 DIR6	P5 DIR5	P5 DIR4	P5 DIR3	P5 DIR2	P5 DIR1	P5 DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

7:0 Each Pin Input/Output of Port 5 0: Input
1: Output

P5DIR : x'00FFE5'

Port 5 Input/Output Control Register

8-bit access register
(16-bit access is possible from even address)

Setting 1 to bits[7:6] and bits[3:0] of this register is not allowed during processor mode.

7	6	5	4	3	2	1	0
-	-	-	-	P6 DIR3	P6 DIR2	P6 DIR1	P6 DIR0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0/1	0/1	0/1	0/1

3:0 Each Pin Input/Output of Port 0: Input
1: Output

P6DIR : x'00FFE6'

Port 6 Input/Output Control Register

8/16-bit access register

Setting 1 to bits[3:1] of this register is not allowed during processor mode.

7	6	5	4	3	2	1	0
*Note	*Note	P7 DIR5	P7 DIR4	P7 DIR3	P7 DIR2	P7 DIR1	P7 DIR0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

*Note: Always set 0.

5:0 Each Pin Input/Output of Port 0: Input
1: Output

P7DIR : x'00FFE7'

Port 7 Input/Output Control Register

8-bit access register
(16-bit access is possible from even address)

7	6	5	4	3	2	1	0
P8 DIR7	P8 DIR6	P8 DIR5	P8 DIR4	P8 DIR3	P8 DIR2	P8 DIR1	P8 DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P8DIR : x'00FFE8'

Port 8 Input/Output Control Register

8/16-bit access register

7:0 Each Pin Input/Output of Port 8 0: Input
1: Output

7	6	5	4	3	2	1	0
P9 DIR7	P9 DIR6	P9 DIR5	P9 DIR4	P9 DIR3	P9 DIR2	P9 DIR1	P9 DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P9DIR : x'00FFE9'

Port 9 Input/Output Control Register

8-bit access register
(16-bit access is possible from even address)

7:0 Each Pin Input/Output of Port 0: Input
1: Output

P

7	6	5	4	3	2	1	0
-	-	PA DIR5	PA DIR4	PA DIR3	PA DIR2	PA DIR1	PA DIR0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0/1	0/1	0/1	0/1	0/1

PADIR : x'00FFEA'

Port A Input/Output Control Register

8/16-bit access register

5:0 Each Pin Input/Output of Port 0: Input
1: Output

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P0 MD0
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0/1

P0MD : x'00FFF0'

Port 0 Output Mode Register

8/16-bit access register

0 **Port 0 Output** 0: P07 to P00 Output
1: D7 to D0 (AD7 to AD0) I/O

P0MD is valid and used as a port when /WORD pin = 'H' and MEMMDn[8] (n=1 to 3) = 'H'.

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P1 MD0
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0/1

P1MD : x'00FFF1'

Port 1 Output Mode Register

8-bit access register
(16-bit access is possible from even address)

0 **Port 1 Output** 0: P17 to P10 Output
1: D15 to D8 (AD15 to AD8) I/O

P1MD is invalid during processor mode.

7	6	5	4	3	2	1	0
-	-	-	P2 MD4	-	-	-	P2 MD0
R	R	R	R/W	R	R	R	R/W
0	0	0	0	0	0	0	0
0	0	0	0/1	0	0	0	0/1

P2MD : x'00FFF2'

Port 2 Output Mode Register

8/16-bit access register

4 **Port 2 Output** 0: P27 to P24 Output
1: A07 to A04 Output

0 **Port 2 Output** 0: P23 to P20 Output
1: A03 to A00 Output

P2MD is invalid in address/data separated mode during processor mode.

7	6	5	4	3	2	1	0
P3 MD7	P3 MD6	P3 MD5	P3 MD4	P3 MD3	P3 MD2	P3 MD1	P3 MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P3MD : x'00FFF3'

Port 3 Output Mode Register

8-bit access register
(16-bit access is possible from even address)

P3MD is invalid in address/data separated mode during processor mode.

7 **Port 3 Output** 0: P37 output 1: A15 output

6 **Port 3 Output** 0: P36 output 1: A14 output

5 **Port 3 Output** 0: P35 output 1: A13 output

4 **Port 3 Output** 0: P34 output 1: A12 output

3 **Port 3 Output** 0: P33 output 1: A11 output

2 **Port 3 Output** 0: P32 output 1: A10 output

1 **Port 3 Output** 0: P31 output 1: A09 output

0 **Port 3 Output** 0: P30 output 1: A08 output

7	6	5	4	3	2	1	0
P4 MD7	P4 MD6	P4 MD5	P4 MD4	P4 MD3	P4 MD2	P4 MD1	P4 MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P4MD : x'00FFF4'

Port 4 Output Mode Register

8/16-bit access register

Bits[5:0] of P4MD are invalid during processor mode.

* Selection is determined by setting with P6MD.

7 **Port 4 Output** 0: P47 output
1: A23 output or WDOUT output*

6 **Port 4 Output** 0: P46 output
1: A22 output or STOP output*

5 **Port 4 Output** 0: P45 output 1: A21 output

4 **Port 4 Output** 0: P44 output 1: A20 output

3 **Port 4 Output** 0: P43 output 1: A19 output

2 **Port 4 Output** 0: P42 output 1: A18 output

1 **Port 4 Output** 0: P41 output 1: A17 output

0 **Port 4 Output** 0: P40 output 1: A16 output

7	6	5	4	3	2	1	0
-	P5 MD6	P5 MD5	P5 MD4	P5 MD3	P5 MD2	P5 MD1	P5 MD0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P5MD : x'00FFF5'

Port 5 Output Mode Register

8-bit access register (16-bit access is possible from even address)

Bits[6, 3:0] of P5MD are invalid during processor mode.

6 **Port 5 Output** 0: P56 output 1: /BSTRE output (address/data separated mode)

5 **Port 5 Output** 0: P56 output 1: ALE (/ALE) output (address/data shared mode)

4 **Port 5 Output** 0: P55 output 1: $\overline{\text{BRACK}}$ output

3 **Port 5 Output** 0: P54 output 1: $\overline{\text{BREQ}}$ Input

2 **Port 5 Output** 0: P53 output 1: $\overline{\text{CS3}}$ output

1 **Port 5 Output** 0: P52 output 1: $\overline{\text{CS2}}$ output

0 **Port 5 Output** 0: P51 output 1: $\overline{\text{CS1}}$ output

0: P50 output 1: $\overline{\text{CS0}}$ output

7	6	5	4	3	2	1	0
P6 MD7	P6 MD6	-	-	P6 MD3	P6 MD2	P6 MD1	-
R/W	R/W	R	R	R/W	R/W	R/W	R
0	0	0	0	0	0	0	0
0/1	0/1	0	0	0/1	0/1	0/1	0

P6MD : x'00FFF6'

Port 6 Output Mode Register

8/16-bit access register

Bits[3:1] of P6MD are invalid during processor mode.

7 **Selection When P6MD7 is High** 0: A23 output 1: WDOUT output

6 **Selection When P6MD6 is High** 0: A22 output 1: STOP output

3 **Port 6 Output** 0: P63 output 1: $\overline{\text{WEH}}$ output

2 **Port 6 Output** 0: P62 output 1: $\overline{\text{WEL}}$ output

1 **Port 6 Output** 0: P61 output 1: $\overline{\text{RE}}$ output

7	6	5	4	3	2	1	0
-	-	P7 MD5	-	P7 MD3	P7 MD2	-	P7 MD0
R	R	R/W	R	R/W	R/W	R	R/W
0	0	0	0	0	0	0	0
0	0	0/1	0	0/1	0/1	0	0/1

P7MD : x'00FFF7'

Port 7 Output Mode Register

8-bit access register
(16-bit access is possible from even address)

5	**Port 7 Output**	0: P75 output	1: SBO1 output
3	**Port 7 Output**	0: P73 output	1: SBT1 output
2	**Port 7 Output**	0: P72 output	1: SBO0 output
0	**Port 7 Output**	0: P70 output	1: SBT0 output

7	6	5	4	3	2	1	0
P8 MD7	P8 MD6	P8 MD5	P8 MD4	P8 MD3	P8 MD2	P8 MD1	P8 MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

P8MD : x'00FFF8'

Port 8 Output Mode Register

8/16-bit access register

7	**Port 8 Output**	0: P87 output	1: TM6IOB output
6	**Port 8 Output**	0: P86 output	1: TM6IOA output
5	**Port 8 Output**	0: P85 output	1: TM5IO output
4	**Port 8 Output**	0: P84 output	1: TM4IO output
3	**Port 8 Output**	0: P83 output	1: TM3IO output
2	**Port 8 Output**	0: P82 output	1: TM2IO output
1	**Port 8 Output**	0: P81 output	1: TM1IO output
0	**Port 8 Output**	0: P80 output	1: TM0IO output

7	6	5	4	3	2	1	0
-	-	-	P9 MD4	P9 MD3	P9 MD2	P9 MD1	-
R	R	R	R/W	R/W	R/W	R/W	R
0	0	0	0	0	0	0	0
0	0	0	0/1	0/1	0/1	0/1	0

P9MD : x'00FFF9'

Port 9 Output Mode Register

8-bit access register
(16-bit access is possible from even address)

4 **LED Drive Selection** 0: Disable 1: Enable

3 **LED Drive Selection** 0: Disable 1: Enable

2 **Port 9 Output** 0: P92 output 1: TM7IOB output

1 **Port 9 Output** 0: P91 output 1: TM7IOA output

P

9-2-2 Address Map

(1/2)

Lower 4bit / Upper 20bit	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Remarks
x'00FC00'	IAGR ◆												MEMCTR ❍		CPUM ❍		Internal control reg.
x'00FC30'									MEMMD3 ❍		MEMMD2 ❍		MEMMD1 ❍		MEMMD0 ❍		Memory register
x'00FC40'	G7ICR ◆ (VCT=14)		G6ICR ◆ (VCT=12)		G5ICR ◆ (VCT=10)		G4ICR ◆ (VCT=8)		G3ICR ◆ (VCT=6)		G2ICR ◆ (VCT=4)		G1ICR ◆ (VCT=2)		G0ICR ◆ (VCT=0)		Interrupt control registers
x'00FC50'															EXTMD ◆		
x'00FD00'															EXMCTR ◆		External memory Control register
x'00FD10'													ATCBC ◆		ATCCTR ◆		ATC registers
x'00FD70'													No Access (See Note)				
x'00FD80'													SC0STR ✲	SC0TRB ◆	SC0CTR ◆		Serial interfaces 2 channels
x'00FD90'													SC1STR ✲	SC1TRB ◆	SC1CTR ◆		
x'00FDA0'	AN7BUF ✲	AN6BUF ◆	AN5BUF ✲	AN4BUF ◆	AN3BUF ✲	AN2BUF ◆	AN1BUF ✲	AN0BUF ◆							ANCTR ◆		A/D converter
x'00FE00'											TM5BC ✲	TM4BC ◆	TM3BC ✲	TM2BC ◆	TM1BC ✲	TM0BC ◆	Timer 8 channels
x'00FE10'											TM5BR ✲	TM4BR ◆	TM3BR ✲	TM2BR ◆	TM1BR ✲	TM0BR ◆	
x'00FE20'											TM5MD ✲	TM4MD ◆	TM3MD ✲	TM2MD ◆	TM1MD ✲	TM0MD ◆	
x'00FE30'							TM6CB ❍				TM6CA ❍		TM6BC ❍		TM6MD ❍		
x'00FE40'							TM7CB ❍				TM7CA ❍		TM7BC ❍		TM7MD ❍		

◆ =8/16-bit access ❍ =16-bit access ✲ =8-bit access (16-bit access is possible from an even address.) No symbol = 8-bit access

Note: x'00FD72' and x'00FD73' are the system reserved area. Accessing those addresses is not allowed. If accessing those areas, the system operation cannot be guaranteed.

Lower 4bit / Upper 20bit	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	Remarks
x'00FFA0'							LBSWPH ◆		LBSWPL ◆			PB SWPH	PBSWPL ◆		WBSWP ◆		I/O port
x'00FFB0'															PPLU ❍		
x'00FFC0'						PAOUT	P9OUT ✲	P8OUT ◆	P7OUT ✲	P6OUT	P5OUT ✲	P4OUT	P3OUT ✲	P2OUT ◆	P1OUT ✲	P0OUT ◆	
x'00FFD0'						PAIN	P9IN ✲	P8N ◆	P7IN ✲	P6IN	P5IN ✲	P4IN	P3IN ✲	P2IN ◆	P1IN ✲	P0IN ◆	
x'00FFE0'						PADIR	P9DIR ✲	P8DIR ◆	P7DIR ✲	P6DIR	P5DIR ✲	P4DIR	P3DIR ✲	P2DIR ◆	P1DIR ✲	P0DIR ◆	
x'00FFF0'							P9MD ✲	P8MD ◆	P7MD ✲	P6MD	P5MD ✲	P4MD	P3MD ✲	P2MD ◆	P1MD ✲	P0MD ◆	

◆ = 8/16-bit access ❍ = 16-bit access ✲ = 8-bit access (16-bit access is possible from an even address.) No symbol = 8-bit access

9-2-3 List of Pin Functions

EE = External excitation

	Pin Name	Input level	Output level	Schmitt trigger	Pull-up register	RESET *1	RESET *2	RESET *3	BREQ="L"	STOP/HALT
1	P60,WAIT	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
2	P61,$\overline{RE}$	TTL	CMOS	Yes	Programmable	Hi-Z	High	High	Hi-Z at $\overline{RE}$	Hi-Z at $\overline{RE}$
3	P62,$\overline{WEL}$	TTL	CMOS	Yes	Programmable	Hi-Z	High	High	Hi-Z at $\overline{WEL}$	Hi-Z at $\overline{WEL}$
4	P63,$\overline{WEH}$	TTL	CMOS	Yes	Programmable	Hi-Z	High	High	Hi-Z at $\overline{WEH}$	Hi-Z at $\overline{WEH}$
5	P50,$\overline{CS0}$	TTL	CMOS	Yes	Programmable	Hi-Z	High	High	Hi-Z at $\overline{CS0}$	Hi-Z at $\overline{CS0}$
6	P51,$\overline{CS1}$	TTL	CMOS	Yes	Programmable	Hi-Z	High	High	Hi-Z at $\overline{CS1}$	Hi-Z at $\overline{CS1}$
7	P52,$\overline{CS2}$	TTL	CMOS	Yes	Programmable	Hi-Z	High	High	Hi-Z at $\overline{CS2}$	Hi-Z at $\overline{CS2}$
8	P53,$\overline{CS3}$	TTL	CMOS	Yes	Programmable	Hi-Z	High	High	Hi-Z at $\overline{CS3}$	Hi-Z at $\overline{CS3}$
9	P54,$\overline{BREQ}$	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	Low	*
10	P55,$\overline{BRACK}$	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	Low	*
11	P56,ALE,$\overline{ALE}$,$\overline{BSTRE}$	TTL	CMOS	Yes	Programmable	Hi-Z	High	High	Hi-Z except P56	Hi-Z except P56
12	P57,$\overline{WORD}$	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
13	P20,A00	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A00	Hi-Z at A00
14	P21,A01	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A01	Hi-Z at A01
15	P22,A02	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A02	Hi-Z at A02
16	P23,A03	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A03	Hi-Z at A03
17	VDD	-	-	-	-	-	-	-	-	-
18	SYSCLK	-	CMOS	-	No	High	High	High	*	*4
19	VSS	-	-	-	-	-	-	-	-	-
20	XI	-	-	-	-	-	-	-	-	-
21	XO	-	-	-	-	High(EE)	High(EE)	High(EE)	*	*4
22	VDD	-	-	-	-	-	-	-	-	-
23	OSCI	-	-	-	-	-	-	-	-	-
24	OSCO	-	-	-	-	High(EE)	High(EE)	High(EE)	*	*5
25	MODE	CMOS	-	Yes	No	High(Input)	Low(Input)	Low(Input)	MODE	MODE
26	P24,A04	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A04	Hi-Z at A04
27	P25,A05	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A05	Hi-Z at A05
28	P26,A06	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A06	Hi-Z at A06
29	P27,A07	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A07	Hi-Z at A07
30	P30,A08	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A08	Hi-Z at A08
31	P31,A09	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A09	Hi-Z at A09
32	P32,A10	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A10	Hi-Z at A10
33	P33,A11	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A11	Hi-Z at A11
34	VDD	-	-	-	-	-	-	-	-	-
35	P34,A12	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A12	Hi-Z at A12
36	P35,A13	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A13	Hi-Z at A13
37	P36,A14	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A14	Hi-Z at A14
38	P37,A15	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A15	Hi-Z at A15
39	P40,A16	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Undefined	Hi-Z at A16	Hi-Z at A16
40	P41,A17	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Undefined	Hi-Z at A17	Hi-Z at A17
41	P42,A18	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Undefined	Hi-Z at A18	Hi-Z at A18
42	P43,A19	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Undefined	Hi-Z at A19	Hi-Z at A19
43	VSS	-	-	-	-	-	-	-	-	-
44	P44,A20,AN4	Analog	CMOS	No	Programmable	Hi-Z	Hi-Z	Undefined	Hi-Z at A20	Hi-Z at A20
45	P45,A21,AN5	Analog	CMOS	No	Programmable	Hi-Z	Hi-Z	Undefined	Hi-Z at A21	Hi-Z at A21
46	P46,A22,STOP,AN6	Analog	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A22	Hi-Z at A22
47	P47,A23,WDOUT,AN7	Analog	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z at A23	Hi-Z at A23
48	P80,TM0IO	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
49	P81,TM1IO	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
50	P82,TM2IO	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*

51	P83,TM3IO	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
52	P84,TM4IO	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
53	P85,TM5IO	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
54	VDD	-	-	-	-	-	-	-	-	-
55	P86,TM6IOA	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
56	P87,TM6IOB	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
57	P90,TM6IC	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
58	P91,TM7IOA	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
59	P92,TM7IOB	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
60	P93,TM7IC	TTL	CMOS	Yes	No	Hi-Z	Hi-Z	Hi-Z	*	*
61	VSS	-	-	-	-	-	-	-	-	-
62	P94,AN0	Analog	CMOS	No	No	Hi-Z	Hi-Z	Hi-Z	*	*
63	P95,AN1	Analog	CMOS	No	No	Hi-Z	Hi-Z	Hi-Z	*	*
64	P96,AN2	Analog	CMOS	No	No	Hi-Z	Hi-Z	Hi-Z	*	*
65	P97,AN3	Analog	CMOS	No	No	Hi-Z	Hi-Z	Hi-Z	*	*
66	VDD(VPP)	-	-	-	-	-	-	-	-	-
67	P70,SBT0	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
68	P71,SBI0	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
69	P72,SBO0	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
70	P73,SBT1	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
71	P74,SBI1	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
72	P75,SBO1	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
73	Pull-up	-	-	-	-	-	-	-	-	-
74	Pull-up	-	-	-	-	-	-	-	-	-
75	$\overline{NMI}$	TTL	-	Yes	No	$\overline{NMI}$	$\overline{NMI}$	$\overline{NMI}$	$\overline{NMI}$	$\overline{NMI}$
76	PA0,$\overline{IRQ0}$	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
77	PA1,$\overline{IRQ1}$	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
78	PA2,$\overline{IRQ2}$	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
79	PA3,$\overline{IRQ3}$	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
80	PA4,$\overline{IRQ4}$	TTL	CMOS	Yes	Programmable	Hi-Z	Hi-Z	Hi-Z	*	*
81	PA5,ADSEP	CMOS	CMOS	Yes	No	Hi-Z	HighInput)	Low(Input)	*	*
82	$\overline{RST}$	CMOS	-	Yes	Always	Low(Input)	Low(Input)	Low(Input)	High	High
83	VDD	-	-	-	-	-	-	-	-	-
84	P00,D00,AD00	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P00	Hi-Z except P00
85	P01,D01,AD01	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P01	Hi-Z except P01
86	P02,D02,AD02	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P02	Hi-Z except P02
87	P03,D03,AD03	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P03	Hi-Z except P03
88	P04,D04,AD04	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P04	Hi-Z except P04
89	P05,D05,AD05	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P05	Hi-Z except P05
90	P06,D06,AD06	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P06	Hi-Z except P06
91	P07,D07,AD07	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P07	Hi-Z except P07
92	VSS	-	-	-	-	-	-	-	-	-
93	P10,D08,AD08	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P10	Hi-Z except P10
94	P11,D09,AD09	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P11	Hi-Z except P11
95	P12,D10,AD10	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P12	Hi-Z except P12
96	P13,D11,AD11	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P13	Hi-Z except P13
97	P14,D12,AD12	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P14	Hi-Z except P14
98	P15,D13,AD13	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P15	Hi-Z except P15
99	P16,D14,AD14	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P16	Hi-Z except P16
100	P17,D15,AD15	TTL	CMOS	No	Programmable	Hi-Z	Hi-Z	Hi-Z	Hi-Z except P17	Hi-Z except P17

*: Depends on pin setting *1: Single-chip mode *2:Processor mode (Address/Data separated mode) *3: Processor mode (Address/Data share mode) *4: High during STOP mode

*5:High during STOP and HALT 1 mode

9-3 Instruction Set

MN102L SERIES INSTRUCTION SET

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
MOV	MOV Dm,An	Dm→An	—	—	—	—	—	—	—	—	—	2	2	F2:30+Dm<<2+An
	MOV An,Dm	An→Dm	—	—	—	—	—	—	—	—	—	2	2	F2:F0+An<<2+Dm
	MOV Dn,Dm	Dn→Dm	—	—	—	—	—	—	—	—	—	1	1	80+Dn<<2+Dm *1
	MOV An,Am	An→Am	—	—	—	—	—	—	—	—	—	2	2	F2:70+An<<2+Am
	MOV PSW,Dn	PSW→Dn	0	—	—	—	—	—	—	—	—	2	2	F3:F0+Dn
	MOV Dn,PSW	Dn→PSW	—	●	●	●	●	●	●	●	●	2	3	F3:D0+Dn<<2
	MOV MDR,Dn	MDR→Dn	0	—	—	—	—	—	—	—	—	2	2	F3:E0+Dn
	MOV Dn,MDR	Dn→MDR	—	—	—	—	—	—	—	—	—	2	2	F3:C0+Dn<<2
	MOV (An),Dm	mem16(An)→Dm	S	—	—	—	—	—	—	—	—	1	1	20+An<<2+Dm
	MOV (d8,An),Dm	mem16(An+d8)→Dm	S	—	—	—	—	—	—	—	—	2	1	60+An<<2+Dm:d8
	MOV (d16,An),Dm	mem16(An+d16)→Dm	S	—	—	—	—	—	—	—	—	4	2	F7:C0+An<<2+Dm:d16-l:d16-h
	MOV (d24,An),Dm	mem16(An+d24)→Dm	S	—	—	—	—	—	—	—	—	5	3	F4:80+An<<2+Dm:d24-l:d24-m:d24-h
	MOV (Di,An),Dm	mem16(An+Di)→Dm	S	—	—	—	—	—	—	—	—	2	2	F1:40+Di<<4+An<<2+Dm
	MOV (abs16),Dn	mem16(abs16)→Dn	S	—	—	—	—	—	—	—	—	3	1	C8+Dn:abs16-l:abs16-h
	MOV (abs24),Dn	mem16(abs24)→Dn	S	—	—	—	—	—	—	—	—	5	3	F4:C0+Dn:abs24-l:abs24-m:abs24-h
	MOV (An),Am	mem24(An)→Am	—	—	—	—	—	—	—	—	—	2	2	70+An<<2+Am:00 *2
	MOV (d8,An),Am	mem24(An+d8)→Am	—	—	—	—	—	—	—	—	—	2	2	70+An<<2+Am:d8
	MOV (d16,An),Am	mem24(An+d16)→Am	—	—	—	—	—	—	—	—	—	4	3	F7:B0+An<<2+Am:d16-l:d16-h
	MOV (d24,An),Am	mem24(An+d24)→Am	—	—	—	—	—	—	—	—	—	5	4	F4:F0+An<<2+Am:d24-l:d24-m:d24-h
	MOV (abs16),An	mem24(abs16)→An	—	—	—	—	—	—	—	—	—	4	3	F7:30+An:abs16-l:abs16-h
	MOV (abs24),An	mem24(abs24)→An	—	—	—	—	—	—	—	—	—	5	4	F4:D0+An:abs24-l:abs24-m:abs24-h
	MOV Dm,(An)	Dm→mem16(An)	—	—	—	—	—	—	—	—	—	1	1	00+An<<2+Dm
	MOV Dm,(d8,An)	Dm→mem16(An+d8)	—	—	—	—	—	—	—	—	—	2	1	40+An<<2+Dm:d8
	MOV Dm,(d16,An)	Dm→mem16(An+d16)	—	—	—	—	—	—	—	—	—	4	2	F7:80+An<<2+Dm:d16-l:d16-h
	MOV Dm,(d24,An)	Dm→mem16(An+d24)	—	—	—	—	—	—	—	—	—	5	3	F4:00+An<<2+Dm:d24-l:d24-m:d24-h
	MOV Dm,(Di,An)	Dm→mem16(An+Di)	—	—	—	—	—	—	—	—	—	2	2	F1:C0+Di<<4+An<<2+Dm
	MOV Dn,(abs16)	Dn→mem16(abs16)	—	—	—	—	—	—	—	—	—	3	1	C0+Dn:abs16-l:abs16-h
	MOV Dn,(abs24)	Dn→mem16(abs24)	—	—	—	—	—	—	—	—	—	5	3	F4:40+Dn:abs24-l:abs24-m:abs24-h
	MOV Am,(An)	Am→mem24(An)	—	—	—	—	—	—	—	—	—	2	2	50+An<<2+Am:00 *3
	MOV Am,(d8,An)	Am→mem24(An+d8)	—	—	—	—	—	—	—	—	—	2	2	50+An<<2+Am:d8
	MOV Am,(d16,An)	Am→mem24(An+d16)	—	—	—	—	—	—	—	—	—	4	3	F7:A0+An<<2+Am:d16-l:d16-h
	MOV Am,(d24,An)	Am→mem24(An+d24)	—	—	—	—	—	—	—	—	—	5	4	F4:10+An<<2+Am:d24-l:d24-m:d24-h
	MOV An,(abs16)	An→mem24(abs16)	—	—	—	—	—	—	—	—	—	4	3	F7:20+An:abs16-l:abs16-h
	MOV An,(abs24)	An→mem24(abs24)	—	—	—	—	—	—	—	—	—	5	4	F4:50+An:abs24-l:abs24-m:abs24-h
	MOV imm8,Dn	imm8→Dn	S	—	—	—	—	—	—	—	—	2	1	80+Dn<<2+Dn:imm8
	MOV imm16,Dn	imm16→Dn	S	—	—	—	—	—	—	—	—	3	1	F8+Dn:imm16-l:imm16-h
	MOV imm24,Dn	imm24→Dn	—	—	—	—	—	—	—	—	—	5	3	F4:70+Dn:imm24-l:imm24-m:imm24-h
	MOV imm16,An	imm16→An	0	—	—	—	—	—	—	—	—	3	1	DC+An:imm16-l:imm16-h
	MOV imm24,An	imm24→An	—	—	—	—	—	—	—	—	—	5	3	F4:74+An:imm24-l:imm24-m:imm24-h
MOVX	MOVX (d8,An),Dm	mem24(An+d8)→Dm	—	—	—	—	—	—	—	—	—	3	3	F5:70+An<<2+Dm:d8
	MOVX (d16,An),Dm	mem24(An+d16)→Dm	—	—	—	—	—	—	—	—	—	4	3	F7:70+An<<2+Dm:d16-l:d16-h
	MOVX (d24,An),Dm	mem24(An+d24)→Dm	—	—	—	—	—	—	—	—	—	5	4	F4:B0+An<<2+Dm:d24-l:d24-m:d24-h
	MOVX Dm,(d8,An)	Dm→mem24(An+d8)	—	—	—	—	—	—	—	—	—	3	3	F5:50+An<<2+Dm:d8
	MOVX Dm,(d16,An)	Dm→mem24(An+d16)	—	—	—	—	—	—	—	—	—	4	3	F7:60+An<<2+Dm:d16-l:d16-h
	MOVX Dm,(d24,An)	Dm→mem24(An+d24)	—	—	—	—	—	—	—	—	—	5	4	F4:30+An<<2+Dm:d24-l:d24-m:d24-h
MOVB	MOVB (An),Dm	mem8(An)→Dm	S	—	—	—	—	—	—	—	—	2	2	30+An<<2+Dm:B8+Dm *4
	MOVB (d8,An),Dm	mem8(An+d8)→Dm	S	—	—	—	—	—	—	—	—	3	2	F5:20+An<<2+Dm:d8
	MOVB (d16,An),Dm	mem8(An+d16)→Dm	S	—	—	—	—	—	—	—	—	4	2	F7:D0+An<<2+Dm:d16-l:d16-h
	MOVB (d24,An),Dm	mem8(An+d24)→Dm	S	—	—	—	—	—	—	—	—	5	3	F4:A0+An<<2+Dm:d24-l:d24-m:d24-h
	MOVB (Di,An),Dm	mem8(An+Di)→Dm	S	—	—	—	—	—	—	—	—	2	2	F0:40+Di<<4+An<<2+Dm
	MOVB (abs16),Dn	mem8(abs16)→Dn	S	—	—	—	—	—	—	—	—	4	2	CC+Dn:abs16-l:abs16--h:B8+Dn *5
	MOVB (abs24),Dn	mem8(abs24)→Dn	S	—	—	—	—	—	—	—	—	5	3	F4:C4+Dn:abs24-l:abs24-m:abs24-h
	MOVB Dm,(An)	Dm→mem8(An)	—	—	—	—	—	—	—	—	—	1	1	10+Dm<<2+An
	MOVB Dm,(d8,An)	Dm→mem8(An+d8)	—	—	—	—	—	—	—	—	—	3	2	F5:10+An<<2+Dm:d8
	MOVB Dm,(d16,An)	Dm→mem8(An+d16)	—	—	—	—	—	—	—	—	—	4	2	F7:90+An<<2+Dm:d16-l:d16-h
	MOVB Dm,(d24,An)	Dm→mem8(An+d24)	—	—	—	—	—	—	—	—	—	5	3	F4:20+An<<2+Dm:d24-l:d24-m:d24-h
	MOVB Dm,(Di,An)	Dm→mem8(An+Di)	—	—	—	—	—	—	—	—	—	2	2	F0:C0+Di<<4+An<<2+Dm

Notes: *1 It is not possible to specify that Dn=Dm.
*2 This instruction is supported by the assembler. For "MOV (d8,An),Am" the assembler will generate a bit pattern for d8=0.
*3 This instruction is supported by the assembler. For "MOV Am,(d8,An)" the assembler will generate a bit pattern for d8=0.
*4 This instruction is supported by the assembler. The assembler generates bit patterns for the two instructions "MOVBU (An),Dm" and "EXTXB Dm".
*5 This instruction is supported by the assembler. The assembler generates bit patterns for the two instructions "MOVBU (abs16),Dn" and "EXTXB Dn".

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
MOVB	MOVB Dn,(abs16)	Dn→mem8(abs16)	—	—	—	—	—	—	—	—	—	3	1	C4+Dn:abs16-l:abs16-h
	MOVB Dn,(abs24)	Dn→mem8(abs24)	—	—	—	—	—	—	—	—	—	5	3	F4:44+Dn:abs24-l:abs24-m:abs24-h
MOVBU	MOVBU (An),Dm	mem8(An)→Dm	0	—	—	—	—	—	—	—	—	1	1	30+An<<2+Dm
	MOVBU (d8,An),Dm	mem8(An+d8)→Dm	0	—	—	—	—	—	—	—	—	3	2	F5:30+An<<2+Dm:d8
	MOVBU (d16,An),Dm	mem8(An+d16)→Dm	0	—	—	—	—	—	—	—	—	4	2	F7:50+An<<2+Dm:d16-l:d16-h
	MOVBU (d24,An),Dm	mem8(An+d24)→Dm	0	—	—	—	—	—	—	—	—	5	3	F4:90+An<<2+Dm:d24-l:d24-m:d24-h
	MOVBU (Di,An),Dm	mem8(An+Di)→Dm	0	—	—	—	—	—	—	—	—	2	2	F0:80+Di<<4+An<<2+Dm
	MOVBU (abs16),Dn	mem8(abs16)→Dn	0	—	—	—	—	—	—	—	—	3	1	CC+Dn:abs16-l:abs16-h
	MOVBU (abs24),Dn	mem8(abs24)→Dn	0	—	—	—	—	—	—	—	—	5	3	F4:C8+Dn:abs24-l:abs24-m:abs24-h
EXT	EXT Dn	IF Dn.bp15=0 x'0000'→MDR IF Dn.bp15=1 x'FFFF'→MDR	S	—	—	—	—	—	—	—	—	2	3	F3:C1+Dn<<2 *6
EXTX	EXTX Dn	IF Dn.bp15=0 Dn&x'00FFFF'→Dn IF Dn.bp15=1 Dn|x'FF0000'→Dn	S	—	—	—	—	—	—	—	—	1	1	B0+Dn *7
EXTXU	EXTXU Dn	Dn&x'00FFFF'→Dn	0	—	—	—	—	—	—	—	—	1	1	B4+Dn *8
EXTXB	EXTXB Dn	IF Dn.bp7=0 Dn&x'0000FF'→Dn IF Dn.bp7=1 Dn|x'FFFF00'→Dn	S	—	—	—	—	—	—	—	—	1	1	B8+Dn *9
EXTXBU	EXTXBU Dn	Dn&x'0000FF'→Dn	0	—	—	—	—	—	—	—	—	1	1	BC+Dn *10
ADD	ADD Dn,Dm	Dm+Dn→Dm	—	●	●	●	●	●	●	●	●	1	1	90+Dn<<2+Dm
	ADD Dm,An	An+Dm→An	—	●	●	●	●	●	●	●	●	2	2	F2:00+Dm<<2+An
	ADD An,Dm	Dm+An→Dm	—	●	●	●	●	●	●	●	●	2	2	F2:C0+An<<2+Dm
	ADD An,Am	Am+An→Am	—	●	●	●	●	●	●	●	●	2	2	F2:40+An<<2+Am
	ADD imm8,Dn	Dn+imm8→Dn	S	●	●	●	●	●	●	●	●	2	1	D4+Dn:imm8
	ADD imm16,Dn	Dn+imm16→Dn	S	●	●	●	●	●	●	●	●	4	2	F7:18+Dn:imm16-l:imm16-h
	ADD imm24,Dn	Dn+imm24→Dn	—	●	●	●	●	●	●	●	●	5	3	F4:60+Dn:imm24-l:imm24-m:imm24-h
	ADD imm8,An	An+imm8→An	S	●	●	●	●	●	●	●	●	2	1	D0+An:imm8
	ADD imm16,An	An+imm16→An	S	●	●	●	●	●	●	●	●	4	2	F7:08+An:imm16-l:imm16-h
	ADD imm24,An	An+imm24→An	—	●	●	●	●	●	●	●	●	5	3	F4:64+An:imm24-l:imm24-m:imm24-h
ADDC	ADDC Dn,Dm	Dm+Dn+CF→Dm	—	●	●	●	●	●	●	●	●	2	2	F2:80+Dn<<2+Dm
ADDNF	ADDNF imm8,An	An+imm8→An	S	—	—	—	—	—	—	—	—	3	2	F5:0C+An:imm8 *11
SUB	SUB Dn,Dm	Dm-Dn→Dm	—	●	●	●	●	●	●	●	●	1	1	A0+Dn<<2+Dm
	SUB Dm,An	An-Dm→An	—	●	●	●	●	●	●	●	●	2	2	F2:10+Dm<<2+An
	SUB An,Dm	Dm-An→Dm	—	●	●	●	●	●	●	●	●	2	2	F2:D0+An<<2+Dm
	SUB An,Am	Am-An→Am	—	●	●	●	●	●	●	●	●	2	2	F2:50+An<<2+Am
	SUB imm16,Dn	Dn-imm16→Dn	S	●	●	●	●	●	●	●	●	4	2	F7:1C+Dn:imm16-l:imm16-h
	SUB imm24,Dn	Dn-imm24→Dn	—	●	●	●	●	●	●	●	●	5	3	F4:68+Dn:imm24-l:imm24-m:imm24-h
	SUB imm16,An	An-imm16→An	S	●	●	●	●	●	●	●	●	4	2	F7:0C+An:imm16-l:imm16-h
	SUB imm24,An	An-imm24→An	—	●	●	●	●	●	●	●	●	5	3	F4:6C+An:imm24-l:imm24-m:imm24-h
SUBC	SUBC Dn,Dm	Dm-Dn-CF→Dm	—	●	●	●	●	●	●	●	●	2	2	F2:90+Dn<<2+Dm
MUL	MUL Dn,Dm	Dm * Dn→Dm (Dm * Dn)>>16→MDR	—	?	?	?	?	0	?	●	●	2	12	F3:40+Dn<<2+Dm *12
MULU	MULU Dn,Dm	Dm * Dn→Dm (Dm * Dn)>>16→MDR	—	?	?	?	?	0	?	●	●	2	12	F3:50+Dn<<2+Dm *13
DIVU	DIVU Dn,Dm	(MDR<<16+Dm)/Dn→Dm ...MDR	—	?	?	0/?	●/?	0/1	?	●/?	●/?	2	13	F3:60+Dn<<2+Dm *14

Notes: *6 32-bit sign extended word data
*7 24-bit sign extended word data
*8 24-bit zero extended word data
*9 24-bit sign extended byte data
*10 24-bit zero extended byte data
*11 Addition without changing flag
*12 16x16 = 32 (signed)
*13 16x16 = 32 (unsigned)
*14 32 16 =16...16(unsigned)

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
CMP	CMP Dn,Dm	Dm-Dn	—	●	●	●	●	●	●	●	●	2	2	F3:90+Dn<<2+Dm
	CMP Dm,An	An-Dm	—	●	●	●	●	●	●	●	●	2	2	F2:20+Dm<<2+An
	CMP An,Dm	Dm-An	—	●	●	●	●	●	●	●	●	2	2	F2:E0+An<<2+Dm
	CMP An,Am	Am-An	—	●	●	●	●	●	●	●	●	2	2	F2:60+An<<2+Am
	CMP imm8,Dn	Dn-imm8	S	●	●	●	●	●	●	●	●	2	1	D8+Dn:imm8
	CMP imm16,Dn	Dn-imm16	S	●	●	●	●	●	●	●	●	4	2	F7:48+Dn:imm16-l:imm16-h
	CMP imm24,Dn	Dn-imm24	—	●	●	●	●	●	●	●	●	5	3	F4:78+Dn:imm24-l:imm24-m:imm24-h
	CMP imm16,An	An-imm16	0	●	●	●	●	●	●	●	●	3	1	EC+An:imm16-l:imm16-h
	CMP imm24,An	An-imm24	—	●	●	●	●	●	●	●	●	5	3	F4:7C+An:imm24-l:imm24-m:imm24-h
AND	AND Dn,Dm	Dm&(x'FF0000' |Dn)→Dm	—	—	—	—	—	0	0	●	●	2	2	F3:00+Dn<<2+Dm *15
	AND imm8,Dn	Dn&(x'FF0000' |imm8)→Dn	0	—	—	—	—	0	0	●	●	3	2	F5:00+Dn:imm8 *15
	AND imm16,Dn	Dn&(x'FF0000' |imm16)→Dn	—	—	—	—	—	0	0	●	●	4	2	F7:00+Dn:imm16-l:imm16-h *15
	AND imm16,PSW	PSW&imm16→PSW	—	●	●	●	●	●	●	●	●	4	3	F7:10:imm16-l:imm16-h *15
OR	OR Dn,Dm	Dm|(Dn&x'00FFFF')→Dm	—	—	—	—	—	0	0	●	●	2	2	F3:10+Dn<<2+Dm *15
	OR imm8,Dn	Dn|imm8→Dn	0	—	—	—	—	0	0	●	●	3	2	F5:08+Dn:imm8 *15
	OR imm16,Dn	Dn|imm16→Dn	—	—	—	—	—	0	0	●	●	4	2	F7:40+Dn:imm16-l:imm16-h *15
	OR imm16,PSW	PSW|imm16→PSW	—	●	●	●	●	●	●	●	●	4	3	F7:14:imm16-l:imm16-h *15
XOR	XOR Dn,Dm	Dm^(x'00FFFF'&Dn)→Dm	—	—	—	—	—	0	0	●	●	2	2	F3:20+Dn<<2+Dm *15
	XOR imm16,Dn	Dn^imm16→Dn	—	—	—	—	—	0	0	●	●	4	2	F7:4C+Dn:imm16-l:imm16-h *15
NOT	NOT Dn	Dn^x'00FFFF'→Dn	—	—	—	—	—	0	0	●	●	2	2	F3:E4+Dn *15
ASR	ASR Dn	Dn.lsb→CF Dn.bp→Dn.bp-1(bp15~1) Dn.bp15→Dn.bp15	—	—	—	—	—	0	●	●	●	2	2	F3:38+Dn *15
LSR	LSR Dn	Dn.lsb→CF Dn.bp→Dn.bp-1(bp15~1) 0→Dn.bp15	—	—	—	—	—	0	●	0	●	2	2	F3:3C+Dn *15
ROR	ROR Dn	Dn.lsb→temp Dn.bp→Dn.bp-1(bp15~1) CF→Dn.bp15 temp→CF	—	—	—	—	—	0	●	●	●	2	2	F3:34+Dn *15
ROL	ROL Dn	Dn.bp15→temp Dn.bp→Dn.bp+1(bp14~0) CF→Dn.lsb temp→CF	—	—	—	—	—	0	●	●	●	2	2	F3:30+Dn *15
BTST	BTST imm8,Dn	Dn&imm8 ... PSW	0	—	—	—	—	0	0	0	●	3	2	F5:04+Dn:imm8
	BTST imm16,Dn	Dn&imm16 ... PSW	0	—	—	—	—	0	0	●	●	4	2	F7:04+Dn:imm16-l:imm16-h
BSET	BSET Dm,(An)	mem8(An)&Dm ... PSW mem8(An)|Dm→mem8(An)	0	—	—	—	—	0	0	0	●	2	5	F0:20+An<<2+Dm *16
BCLR	BCLR Dm,(An)	mem8(An)&Dm ... PSW mem8(An)&(¯Dm)→mem8(An)	0	—	—	—	—	0	0	0	●	2	5	F0:30+An<<2+Dm *16
Bcc	BEQ label	IF ZF=1 PC+2+d8(label)→PC IF ZF=0 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E8:d8 *17
	BNE label	IF ZF=0 PC+2+d8(label)→PC IF ZF=1 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E9:d8 *18
	BLT label	IF (VF^NF)=1 PC+2+d8(label)→PC IF (VF^NF)=0 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E0:d8 *19

Notes: *15 16-bit computation
*16 Performed under the conditions of bus lock and disabled interrupts.
*17 src=dest (lower 16 bits)
*18 src≠dest (lower 16 bits)
*19 src>dest (lower 16 bits, signed)

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
Bcc	BLE label	IF ((VF^NF)|ZF)=1 PC+2+d8(label)→PC IF ((VF^NF)|ZF)=0 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E3:d8 *20
	BGE label	IF (VF^NF)=0 PC+2+d8(label)→PC IF (VF^NF)=1 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E2:d8 *21
	BGT label	IF ((VF^NF)|ZF)=0 PC+2+d8(label)→PC IF ((VF^NF)|ZF)=1 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E1:d8 *22
	BCS label	IF CF=1 PC+2+d8(label)→PC IF CF=0 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E4:d8 *23
	BLS label	IF (CF|ZF)=1 PC+2+d8(label)→PC IF (CF|ZF)=0 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E7:d8 *24
	BCC label	IF CF=0 PC+2+d8(label)→PC IF CF=1 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E6:d8 *25
	BHI label	IF (CF|ZF)=0 PC+2+d8(label)→PC IF (CF|ZF)=1 PC+2→PC	—	—	—	—	—	—	—	—	—	2	2/1	E5:d8 *26
	BVC label	IF VF=0 PC+3+d8(label)→PC IF VF=1 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:FC:d8 *27
	BVS label	IF VF=1 PC+3+d8(label)→PC IF VF=0 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:FD:d8 *28
	BNC label	IF NF=0 PC+3+d8(label)→PC IF NF=1 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:FE:d8 *29
	BNS label	IF NF=1 PC+3+d8(label)→PC IF NF=0 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:FF:d8 *30
	BRA label	PC+2+d8(label)→PC	—	—	—	—	—	—	—	—	—	2	2	EA:d8
Bccx	BEQX label	IF ZX=1 PC+3+d8(label)→PC IF ZX=0 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E8:d8 *31
	BNEX label	IF ZX=0 PC+3+d8(label)→PC IF ZX=1 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E9:d8 *32

Notes: *20 src≥dest (lower 16 bits, signed)
*21 src≤dest (lower 16 bits, signed)
*22 src<dest (lower 16 bits, signed)
*23 src>dest (lower 16 bits, unsigned)
*24 src≥dest (lower 16 bits, unsigned)
*25 src≤dest (lower 16 bits, unsigned)
*26 src<dest (lower 16 bits, unsigned)
*27 VF=0
*28 VF=1
*29 NF=0
*30 NF=1
*31 src=dest (24 bits)
*32 src≠dest (24 bits)

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
Bccx	BLTX label	IF (VX^NX)=1 PC+3+d8(label)→PC IF (VX^NX)=0 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E0:d8 *33
	BLEX label	IF ((VX^NX)|ZX)=1 PC+3+d8(label)→PC IF ((VX^NX)|ZX)=0 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E3:d8 *34
	BGEX label	IF (VX^NX)=0 PC+3+d8(label)→PC IF (VX^NX)=1 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E2:d8 *35
	BGTX label	IF ((VX^NX)|ZX)=0 PC+3+d8(label)→PC IF ((VX^NX)|ZX)=1 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E1:d8 *36
	BCSX label	IF CX=1 PC+3+d8(label)→PC IF CX=0 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E4:d8 *37
	BLSX label	IF (CX|ZX)=1 PC+3+d8(label)→PC IF (CX|ZX)=0 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E7:d8 *38
	BCCX label	IF CX=0 PC+3+d8(label)→PC IF CX=1 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E6:d8 *39
	BHIX label	IF (CX|ZX)=0 PC+3+d8(label)→PC IF (CX|ZX)=1 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:E5:d8 *40
	BVCX label	IF VX=0 PC+3+d8(label)→PC IF VX=1 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:EC:d8 *41
	BVSX label	IF VX=1 PC+3+d8(label)→PC IF VX=0 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:ED:d8 *42
	BNCX label	IF NX=0 PC+3+d8(label)→PC IF NX=1 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:EE:d8 *43
	BNSX label	IF NX=1 PC+3+d8(label)→PC IF NX=0 PC+3→PC	—	—	—	—	—	—	—	—	—	3	3/2	F5:EF:d8 *44
JMP	JMP label16	PC+3+d16(label16)→PC	—	—	—	—	—	—	—	—	—	3	2	FC:d16-l:d16-h
	JMP label24	PC+5+d24(label24)→PC	—	—	—	—	—	—	—	—	—	5	4	F4:E0:d24-l:d24-m:d24-h
	JMP (An)	An→PC	—	—	—	—	—	—	—	—	—	2	3	F0:An<<2

Notes: *33 src>dest (24 bits, signed)
*34 src≥dest (24 bits, signed)
*35 src≤dest (24 bits, signed)
*36 src<dest (24 bits, signed)
*37 src>dest (24 bits, unsigned)
*38 src≥dest (24 bits, unsigned)
*39 src≤dest (24 bits, unsigned)
*40 src<dest (24 bits, unsigned)
*41 VX=0
*42 VX=1
*43 NX=0
*44 NX=1

Instruction	Mnemonic	Operation	OP EX.	Flag								Code Size	Cycle	Machine Code
				VX	CX	NX	ZX	VF	CF	NF	ZF			
JSR	JSR label16	A3-4→A3 PC+3→mem24(A3) PC+3+d16(label16)→PC	—	—	—	—	—	—	—	—	—	3	4	FD:d16-l:d16-h
	JSR label24	A3-4→A3 PC+5→mem24(A3) PC+5+d24(label24)→PC	—	—	—	—	—	—	—	—	—	5	5	F4:E1:d24-l:d24-m:d24-h
	JSR (An)	A3-4→A3 PC+2→mem24(A3) An→PC	—	—	—	—	—	—	—	—	—	2	5	F0:01+An<<2
NOP	NOP	PC+1→PC	—	—	—	—	—	—	—	—	—	1	1	F6
RTS	RTS	mem24(A3)→PC A3+4→A3	—	—	—	—	—	—	—	—	—	1	5	FE
RTI	RTI	mem16(A3)→PSW mem24(A3+2)→PC A3+6→A3	—	●	●	●	●	●	●	●	●	1	6	EB

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Reading the instruction set

■ Symbols used in tables

Dn, Dm, Di	Data register
An, Am	Address register
MDR, PSW, PC	Multiply/Divide Register, Processor Status Word, Program Counter
imm8, imm16, imm16-l, imm16-h imm24, imm24-l, imm24-m, imm24-h	Constant
d8, d16, d16-l, d16-h d24, d24-l, d24-m, d24-h	Displacement
abs16, abs16-l, abs16-h abs24, abs24-l, abs24-m, abs24-h	Absolute address
mem8 (An), mem8 (abs16), mem8 (abs24)	8-bit memory data which is determined by the address inside parentheses ( )
mem16 (An), mem16 (abs16), mem16 (abs24)	16-bit memory data which is determined by the address inside parentheses ( )
mem24 (Am), mem24 (abs16), mem24 (abs24)	24-bit memory data which is determined by the address inside parentheses ( )
.bp,.lsb, .msb	Bit specification
&, l , ^	Logical AND, logical OR, exclusive OR
~, <<	Bit inversion, bit shift
VX, CX, NX, ZX,	Extended overflow flag, carry flag, negative flag, zero flag (24-bit data)
VF, CF, NF, ZF	Overflow flag, carry flag, negative flag, zero flag (16-bit data)
temp	CPU internal temporary register
→ , ...	Substitution, reflects calculation results

■ OP EX. (Operand Extensions)

0	Zero-extension
S	Sign-extension
—	Not applicable

■ Flag

●	Changes
—	No change
0	Always 0
1	Always 1
?	Undefined

■ Code Size

Unit : bytes

■ Cycle

Minimum cycle count is shown.

Units : machine cycles

a/b : a cycles if branch taken
b cycles if branch not taken

■ Machine Code

":" indicates a delimiter between bytes.<<2 indicates a 2-bit shift.

Dn, Dm, Di, An, Am : Register numbers

D0	00	A0	00
D1	01	A1	01
D2	10	A2	10
D3	11	A3	11

■ Notes

16-bit or 24-bit access instruction must not access odd memory addresses.
8-bit displacements (d8) and 16-bit displacements (d16) are all sign-extended.

9-4 Instruction Map

MN102L SERIES INSTRUCTION MAP

First byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV Dm, (An)															
1	MOVB Dm, (An)															
2	MOV (An), Dm															
3	MOVBU (An), Dm															
4	MOV Dm, (d8, An)															
5	MOV Am, (d8, An)															
6	MOV (d8, An), Dm															
7	MOV (d8, An), Am															
8	MOV Dn, Dm, (when src=dest,MOV imm8, Dn)															
9	ADD Dn, Dm															
A	SUB Dn, Dm															
B	EXTX Dn				EXTXU Dn				EXTXB Dn				EXTXBU Dn			
C	MOV Dn, (abs16)				MOVB Dn, (abs16)				MOV (abs16),Dn				MOVBU (abs16),Dn			
D	ADD imm8, An				ADD imm8, Dn				CMP imm8, Dn				MOV imm16, An			
E	BLT label	BGT label	BGE label	BLE label	BCS label	BHI label	BCC label	BLS label	BEQ label	BNE label	BRA label	RTI	CMP imm16, An			
F	Extended code (2 bytes)				Extended code (5 bytes)	Extended code (3 bytes)	NOP	Extended code (4 bytes)	MOV imm16, Dn				JMP label16	JSR label16	RTS	

2-byte instructions (Byte 1: F0)

Second byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP (A0)	JSR (A0)			JMP (A1)	JSR (A1)			JMP (A2)	JSR (A2)			JMP (A3)	JSR (A3)		
1																
2	BSET Dm, (An)															
3	BCLR Dm, (An)															
4	MOVB (Di, An), Dm															
5																
6																
7																
8	MOVBU (Di, An), Dm															
9																
A																
B																
C	MOVB Dm, (Di, An)															
D																
E																
F																

2-byte instructions (Byte 1: F1)

Second byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4		MOV (Di, An), Dm														
5																
6																
7																
8																
9																
A																
B																
C		MOV Dm, (Di, An)														
D																
E																
F																

2-byte instructions (Byte 1: F2)

Second byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		ADD Dm, An														
1		SUB Dm, An														
2		CMP Dm, An														
3		MOV Dm, An														
4		ADD An, Am														
5		SUB An, Am														
6		CMP An, Am														
7		MOV An, Am														
8		ADDC Dn, Dm														
9		SUBC Dn, Dm														
A																
B																
C		ADD An, Dm														
D		SUB An, Dm														
E		CMP An, Dm														
F		MOV An, Dm														

2-byte instructions (Byte 1: F3)

Second byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND Dn, Dm															
1	OR Dn, Dm															
2	XOR Dn, Dm															
3	ROL Dn				ROR Dn				ASR Dn				LSR Dn			
4	MUL Dn, Dm															
5	MULU Dn, Dm															
6	DIVU Dn, Dm															
7																
8																
9	CMP Dn, Dm															
A																
B																
C	MOV D0, MDR	EXT D0			MOV D1, MDR	EXT D1			MOV D2, MDR	EXT D2			MOV D3, MDR	EXT D3		
D	MOV D0, PSW				MOV D1, PSW				MOV D2, PSW				MOV D3, PSW			
E	MOV MDR, Dn				NOT Dn											
F	MOV PSW, Dn															

5-byte instructions (Byte 1: F4)

Second byte Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOV Dm, (d24, An)															
1	MOV Am, (d24, An)															
2	MOVB Dm, (d24, An)															
3	MOVX Dm, (d24, An)															
4	MOV Dn, (abs24)				MOVB Dn, (abs24)											
5	MOV An, (abs24)															
6	ADD imm24, Dn				ADD imm24, An				SUB imm24, Dn				SUB imm24, An			
7	MOV imm24, Dn				MOV imm24, An				CMP imm24, Dn				CMP imm24, An			
8	MOV (d24, An), Dm															
9	MOVBU (d24, An), Dm															
A	MOVB (d24, An), Dm															
B	MOVX (d24, An), Dm															
C	MOV (abs24), Dn				MOVB (abs24), Dn				MOVBU (abs24), Dn							
D	MOV (abs24), An															
E	JMP label24	JSR label24														
F	MOV (d24, An), Am															

3-byte instructions (Byte 1: F5)

Second byte / Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND imm8, Dn				BTST imm8, Dn				OR imm8, Dn				ADDNF imm8, An			
1	MOVB Dm, (d8, An)															
2	MOVB (d8, An), Dm															
3	MOVBU (d8, An), Dm															
4																
5	MOVX Dm, (d8, An)															
6																
7	MOVX (d8, An), Dm															
8																
9																
A																
B																
C																
D																
E	BLTX label	BGTX label	BGEX label	BLEX label	BCSX label	BHIX label	BCCX label	BLSX label	BEQX label	BNEX label			BVCX label	BVSX label	BNCX label	BNSX label
F													BVC label	BVS label	BNC label	BNS label

4-byte instructions (Byte 1: F7)

Second byte / Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND imm16, Dn				BTST imm16, Dn				ADD imm16, An				SUB imm16, An			
1	AND imm16 PSW				OR imm16 PSW				ADD imm16, Dn				SUB imm16, Dn			
2	MOV An, (abs16)															
3	MOV (abs16), An															
4	OR imm16, Dn								CMP imm16, Dn				XOR imm16, Dn			
5	MOVBU (d16, An), Dm															
6	MOVX Dm ,(d16, An)															
7	MOVX (d16, An), Dm															
8	MOV Dm, (d16, An)															
9	MOVB Dm, (d16, An)															
A	MOV Am, (d16, An)															
B	MOV (d16, An), Am															
C	MOV (d16, An), Dm															
D	MOVB (d16, An), Dm															
E																
F																

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9-5 Initialization Program

After reset, the initialization program must be located in the CS0 area (x'010000' to x'3FFFFF). In the initialization program, set the number of wait cycles for Block 0 to the MEMMD0 register. Next, set the MEMCTR register. Always set bits [8:0] of the MEMCTR register to '100'. The number of wait cycles set in the MEMMD0 register is valid after setting the MEMCTR register.

Setting the MEMMD0 register and the MEMCTR register must follow this step. If this step is not followed, writing to the MEMCTR register cannot be guaranteed.

Recommend to write x'0410' to MEMCTR_INIT.

In the program, the following symbols and register addresses are equivalent.
(Amemctr) = (x'FC02')
(Amemmd0) = (x'FC30')
(Amemmd1) = (x'FC32')
(Amemmd2) = (x'FC34')
(Amemmd3) = (x'FC36')
(Aexmctr) = (x'FD00')
(Ap01md) = (x'FFF0')
(Ap01dir) = (x'FFE0')
(Ap23md) = (x'FFF2')
(Ap23dir) = (x'FFE2')
(Ap45md) = (x'FFF4')
(Ap45dir) = (x'FFE4')
(Ap6md) = (x'FFF6')
(Ap6dir) = (x'FFE6')

```
; Initialization Program
init    equ   *

; Memory Mode Setting for Block 0
        mov   MEM0_INIT,d0
        mov   d0,(Amemmd0)

; Handshake Mode Setting
        mov   MEMCTR_INIT,d0
        mov   d0,(Amemctr)

; Pin Setting in Memory Expansion
Mode or Processor Mode
        mov   P01M_INIT,d0
        mov   d0,(Ap01md)
        mov   P01D_INIT,d0
        mov   d0,(Ap01dir)
        mov   P23M_INIT,d0
        mov   d0,(Ap23md)
        mov   P23D_INIT,d0
        mov   d0,(Ap23dir)
        mov   P45M_INIT,d0
        mov   d0,(Ap45md)
        mov   P45D_INIT,d0
        mov   d0,(Ap45dir)
        mov   P6M_INIT,d0
        movb  d0,(Ap6md)
        mov   P6D_INIT,d0
        movb  d0,(Ap6dir)

; Memory Mode Setting for Block1,
Block2, Block 3
        mov   MEM1_INIT,d0
        mov   d0,(Amemmd1)
        mov   MEM2_INIT,d0
        mov   d0,(Amemmd2)
        mov   MEM3_INIT,d0
        mov   d0,(Amemmd3)

; Burst ROM Setting
        mov   EXMEM_INIT,d0
        mov   d0,(Aexmctr)
```

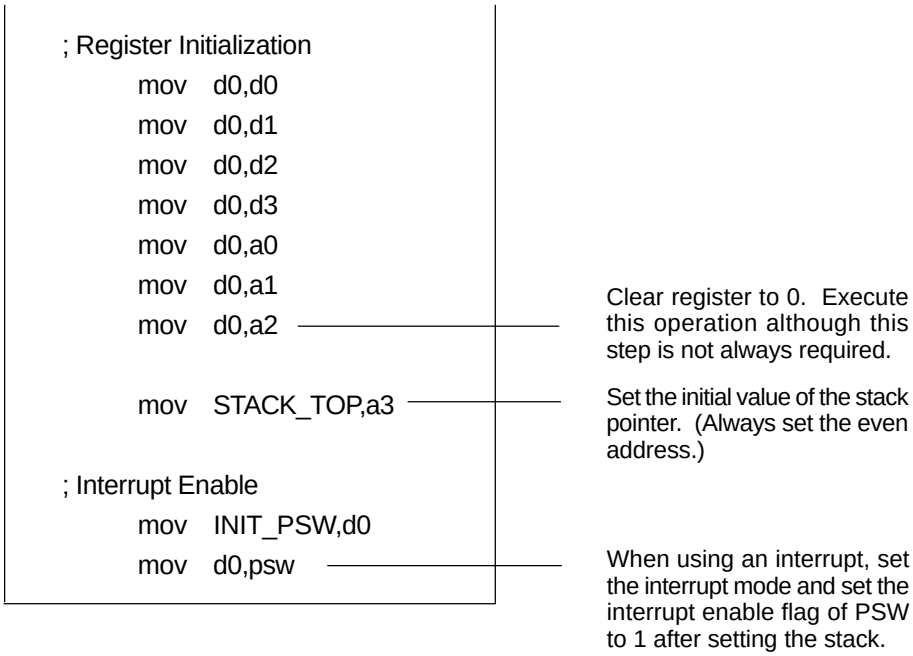
Set the number of wait cycles for block 0 to the MEMMD0 register.

Set bit 10 (HSWTIOE), bit 9 (NWAITIOE) and bit 8 (WAITSET) of the MEMCTR register to 1, 0 and 0 respectively.

Set pins.

Set the number of wait cycles for each block to the associated MEMMDn register. (n=1,2,3)

Set the EXMCTR register when the burst ROM is used, the ALE signal polarity is changed, the pulse width of write enable signal is shortened.


; Register Initialization
mov d0,d0
mov d0,d1
mov d0,d2
mov d0,d3
mov d0,a0
mov d0,a1
mov d0,a2
mov STACK_TOP,a3
; Interrupt Enable
mov INIT_PSW,d0
mov d0,psw
Clear register to 0. Execute this operation although this step is not always required.
Set the initial value of the stack pointer. (Always set the even address.)
When using an interrupt, set the interrupt mode and set the interrupt enable flag of PSW to 1 after setting the stack.

9-6 Flash EEPROM Version

9-6-1 Overview

MN102LF61G is equivalent to MN102L610B with 128 KB of internal Flash EEPROM, which is capable of being programmed /erased electrically.

MN102LF61G is programmed in one of two modes;
PROM writer mode, which uses a dedicated PROM writer for a microcontroller's stand-alone programming. Onboard programming mode, which the CPU controls programming of a microcontroller on a target board.

The 128 KB flash EEPROM is divided into two main areas.

❒ Load program area (6 KB : #0x80000 to #0x817FF)
This area stores a load program for onboard programming mode. This area is overwritten only in PROM writer mode. This area is write/erase-protected in the hardware during onboard programming mode.

❒ User program area (122 KB : #0x81800 to #0x9FFFF)
This area stores an user program. It is overwritten in both programming modes.

Normal operation is guaranteed with up to ten programmings.

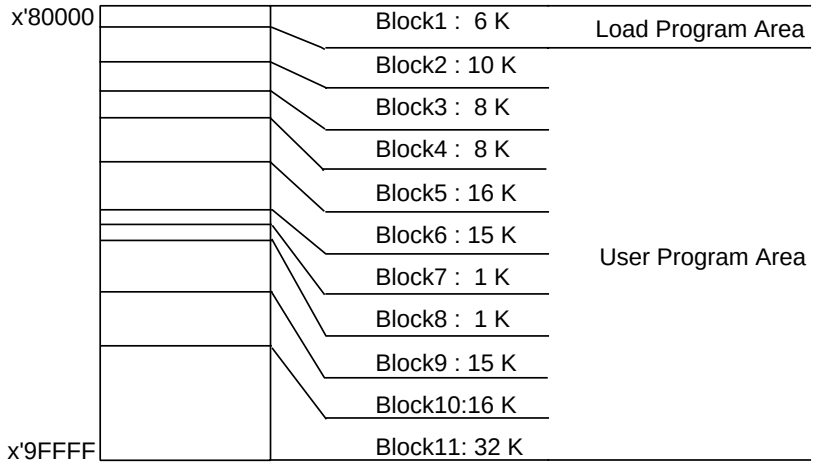


Figure 9-6-1 Memory Map of Internal Flash EEPROM

9-6-2 Reprogramming Flow

Figure 9-6-2 shows the flow for reprogramming (erasing and programming) the flash memory.

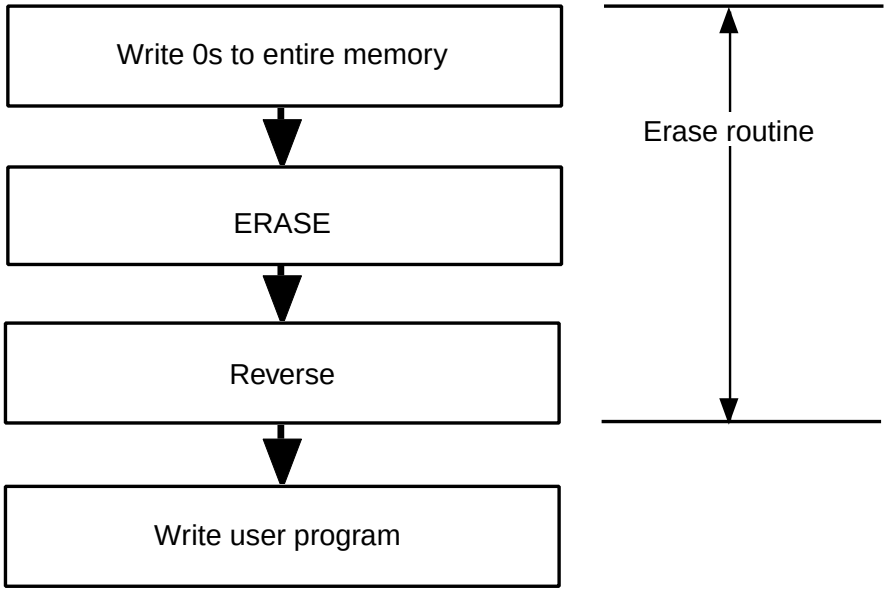


Figure 9-6-2 Internal EEPROM Programming Flow

As the figure shows, the write occurs after the memory is completely erased. The erase routine consists of three steps, first writing all zeros to the entire memory space, next erasing the memory, and finally reversing.

9-6-3 PROM Writer Programming Mode

In PROM writer mode, the CPU is halted for Internal flash EEPROM to be programed. Use the dedicated adaptor socket, which connects to the dedicated PROM writer. When the mocrocontroller connects to the adaptor socket, it automatically enters PROM writer mode.

9-6-4 Onboard Serial Programming Mode

The onboard serial programming mode is primarily used to program the flash EEPROM in devices that are already installed on a PCB board with internal serial interface. Use the dedicated serial writer for programming controlled by the load program. In this mode, load program is write/erase-protected in the hardware.

When you use the YDC serial writer, follow the instructions. Standard onboard serial programming writer comes with load program.

9-6-5 Hardware requirements

1. I/F
Hardware for flash ROM programming on this LSI are as follows.

●8-bit serial interface : 1 set
- ・Data transmission/reception
- ・Transfer bit LSB first
- ・Clock speed over 10 MHz (max.)
- ・Input/output through positive logic

●Input/output pin : 2 pins
- ・SBT and SBD pins for serial I/F

2. I/F Block Diagram

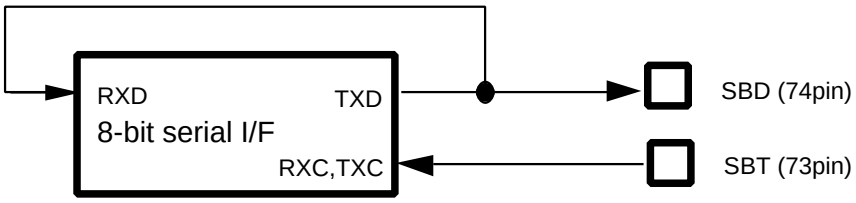


Figure 9-6-3 8-bit Serial Interface Block Diagram

3. Internal flash EEPROM address space

Address	Size	Description
0x80000 | 0x817FF	6 KB	Serial writer load program area
0x81800 | 0x81807	8 bytes	Reserved
0x81808	8 bytes	Reset start
0x81810	8 bytes	Interrupt address
0x81818 | 0x9FFFF	121 KB	User program area

Figure 9-6-4 Internal flash EEPROM address space

1) Serial writer load program area
・These 6 KB of ROM, starting at address 0x80000, holds the load program for the serial writer. This area is write/erase-protected in the hardware.

2) Branch instruction to reset service routine
・Normally, reset servicing starts at address 0x80000, but the soft branch instruction in the serial writer load program branches to 0x81808. This adress must hold a JMP instruction pointing to the real start address for the reset service routine.

3) Branch instruction to interrupt service routine
・Normally, interrupt servicing starts at address 0x80008, but the soft branch instruction in the serial writer load program branches to 0x81810. This adress must hold a JMP instruction pointing to the real start address for the reset service routine.

4) User program area
・This area holds user program.

4. Internal flash EEPROM address space

■Flash serial programming control register

Register: FCREG
Address : x'00FF70'
Use : Control of internal flash EEPROM programming

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit											NRE	RSTIO	EE	NPGM	NOE	NCE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Description
0	Chip enable
1	Output enable
2	Programming
3	Erase enable
4	Flash EEPROM reset
5	Programming enable
15-6	Reserved

■Flash serial programming enable register

Register: FBEWER
Address : x'00FF78'
Use : Enabling of internal flash EPROM programming

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit									BEW7	BEW6	BEW5	BEW4	BEW3	BEW2	BEW1	BEW0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Description
7-0	Serial programming is enable when "01001011" is set Serial programming is disable with other than this setup
15-8	Unpopulated

■Flash address register

Register: FAREG
Address : x'00FF74'
Use : Addressing register for internal flash EEPROM serial programming.
It addresses erase block

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit	FAREG15	FAREG14	FAREG13	FAREG15	FAREG11	FAREG10	FAREG9	FAREG8	FAREG7	FAREG6	FAREG5	FAREG4	FAREG3	FAREG2	FAREG1	FAREG0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0

bit	Description
0	Unpopulated
15-1	Address 15 to 1 bit

Register: FAREGEX
Address : x'00FF76'
Use : Addressing register for internal flash EEPROM serial programming.

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit																FAREG16
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

bit	Description
0	Address 16 bit
7-1	Reserved
15-8	Unpopulated

■Flash data register

Register: FDREG
Address : x'00FF72'
Use : Addressing register for internal flash EEPROM serial programming.

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit	FDREG15	FDREG14	FDREG13	FDREG15	FDREG11	FDREG10	FDREG9	FDREG8	FDREG7	FDREG6	FDREG5	FDREG4	FDREG3	FDREG2	FDREG1	FDREG0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

bit	Description
15-0	Address 15 to 0 bit

9-6-6 Pin Configuration in Onboard Serial Programming

This section describes pin configuration for YDC serial writer.
All input/output pins are input pins at reset release.

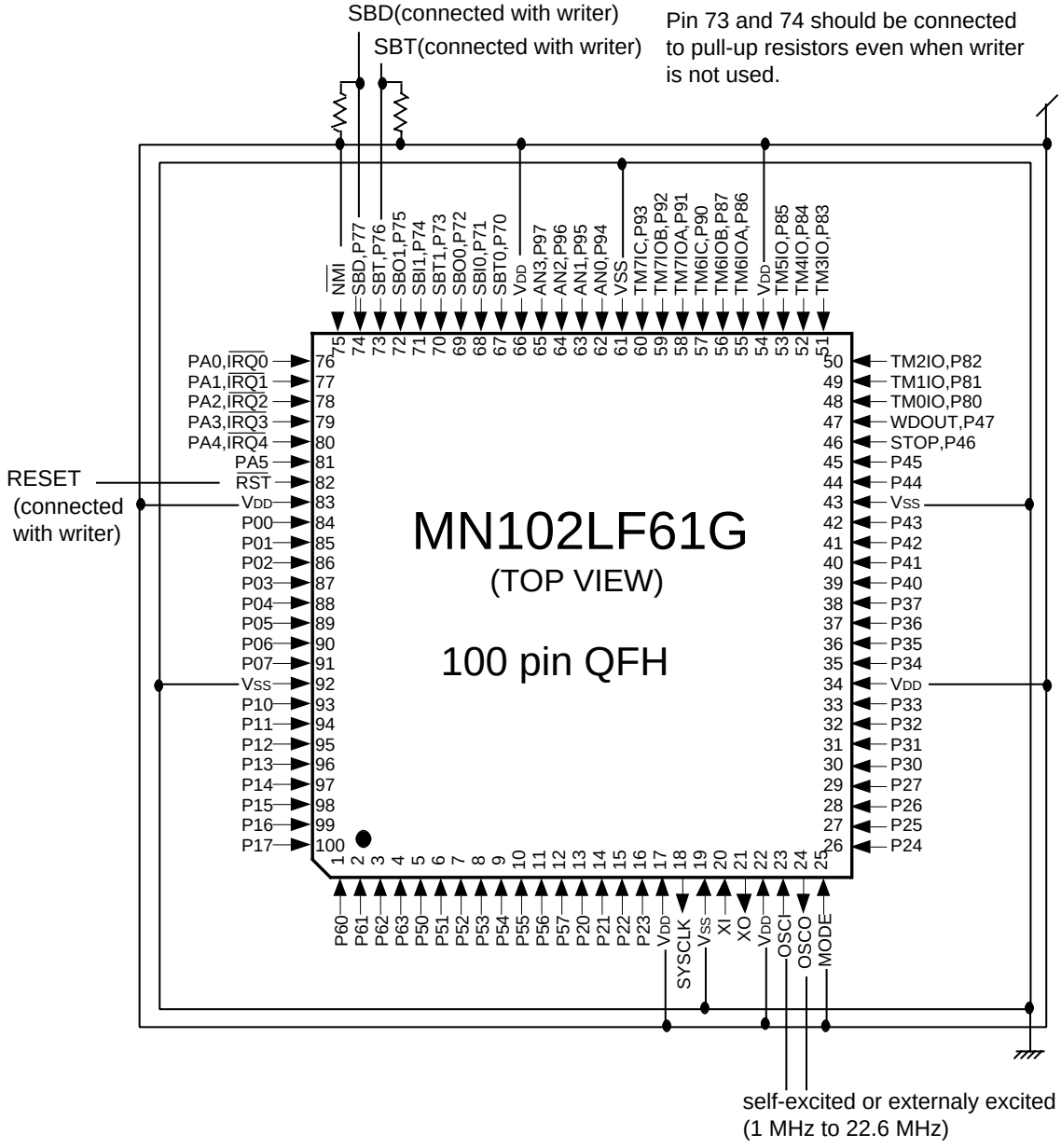

SBD(connected with writer)
SBT(connected with writer)
Pin 73 and 74 should be connected to pull-up resistors even when writer is not used.
MN102LF61G
(TOP VIEW)
100 pin QFH
RESET (connected with writer)
self-excited or externaly excited (1 MHz to 22.6 MHz)

Figure 9-6-5 Pin Configuration for Serial Programming

Connect 73, 74 and 82 pins to the serial writer.
Connect V_{DD} and Vss to 5 V and 0 V power supply.
Output V_{DD} and Vss to the writer, which determines the voltage level.
Set OSCI and OSCO to self-excited or separately externaly excited.
Input pins without connection instruction are ‘Don’t care’ pins, and fix these pins to V_{DD} or Vss.
Leave output pins without connection instruction to OPEN.

9-6-7 Configuring the System for Onboard Serial Programming

1. Entire system configuration

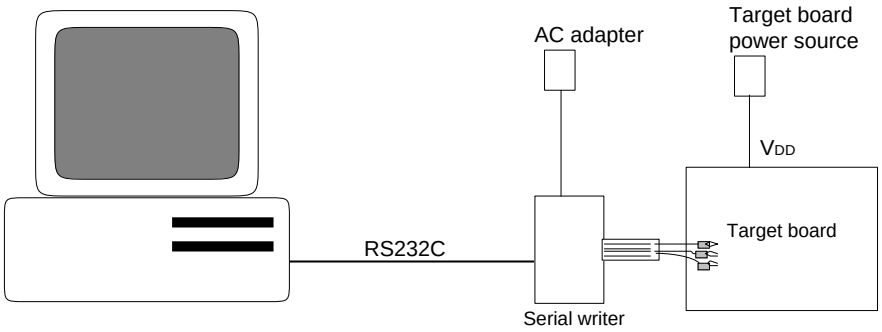


Figure 9-6-6 Configuring System for Onboard Serial Programming

・The pc containing the program data sends the program to the serial writer through RS-232C.
・Through serial communication, the serial writer programs the flash memory inside the microcontroller on the target board.
・VDD source is necessary only when it supplied to the target board.

2. Target board - serial writer connection

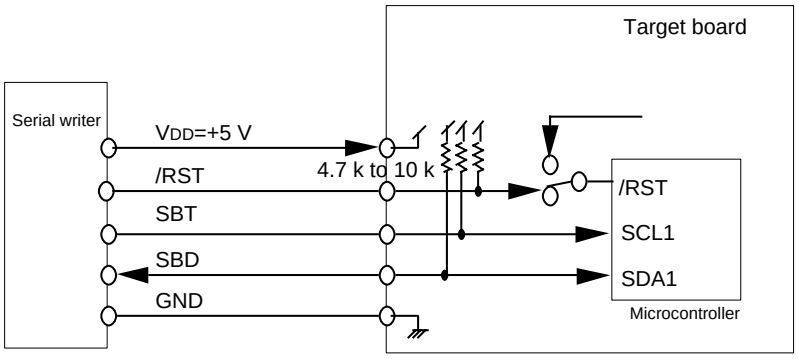


Figure 9-6-7 Pin Configuration on the Target Board

3.Pins

- ●VDD : 4.5 V to 5.5 V power supply (External power)
- ●VDD (level detection) Target board VDD level detection pin
- ●$\overline{\text{RST}}$: Reset
- ●SBT : Clock supply pin for serial interface
- ●SBD : Data input pin for serial interface
- ●GND : Ground

・When VDD is too low, serial writer supplies power to the target board for programming. When VDD level is too low, serial writer generates error message.
・NRST pin outputs microcontroller reset signal.
・Connect pull-up resistors on the target board to NRST, SBT, SBD pins, which are connected to the power supply. The pull-up resistance should be 4.7 kΩ ± 0.47 kΩ (min) to 10 kΩ ± 1 kΩ (max).
・NRST, SBT, SBD pins are output from the serial writer through an open connection.

4.Microcontroller clock on the target board

· For the clock supply to the microcontroler on the target board, use the existing target board clock. Therefore, each user uses different oscillator frequency for the microcontroller clock.
· Following table shows maximum / minimum rating of the oscillator frequency for the microcontroller clock.

Clock frequency Max.	Clock frequency Min.	Target power
22.6 MHz	1.0 MHz	4.5 V to 5.5 V

Table 9-6-1 Maximum / minimum rating of the Oscillator Frequency

9-6-8 On-board Programming Mode Setup

1. Onboard programming mode setup

To enter serial programming mode, the microcontroller must be in write mode.

This section describes the pin setup for the serial writer interface.

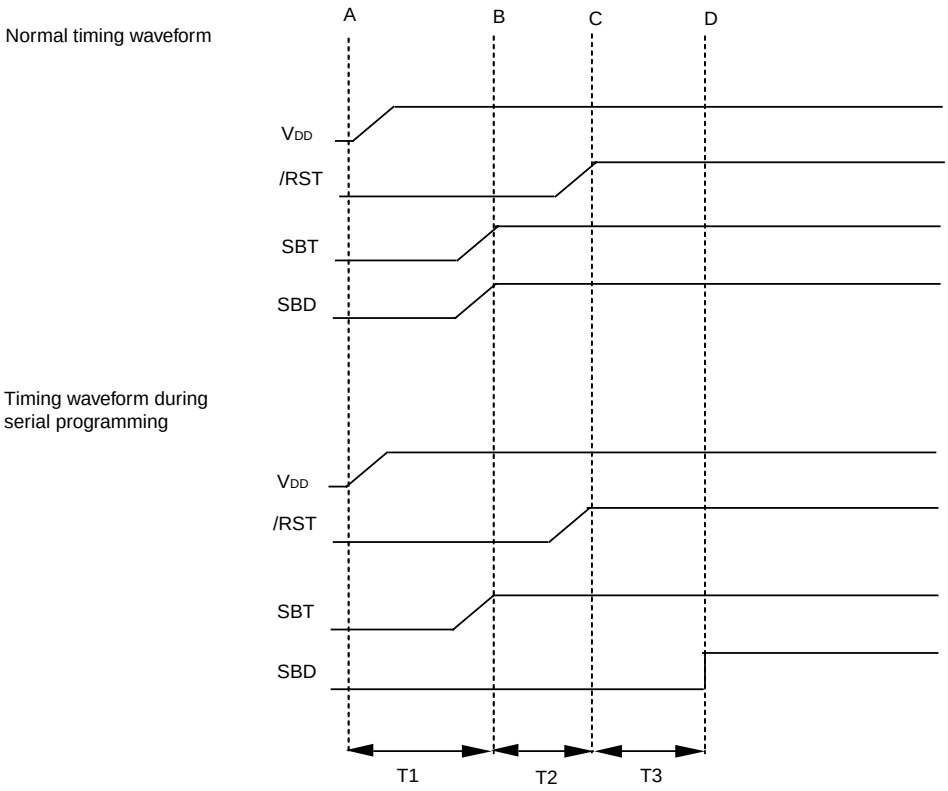


Figure 9-6-8 Timing Waveform during Serial Programming

●To set up the serial writer interface:

1. At timing A, serial interface writer supplies V_{DD}, and at this time, it outputs NRST=SBD=Low.
2. Through the serial writer, drive the NRST pin from timing B, when SBT goes high on microcontroller power-up, for T2 cycles. The microcontroller initializes.
3. Through the serial writer, drive the NRST pin Low from time C, when SBD goes high on microcontroller power-up, for T3 cycles. This signals the microcontroller that it is connected to the serial writer.
4. Make T3 long enough to allow the microcontroller oscillator to stabilize.

●Start routine for the load program

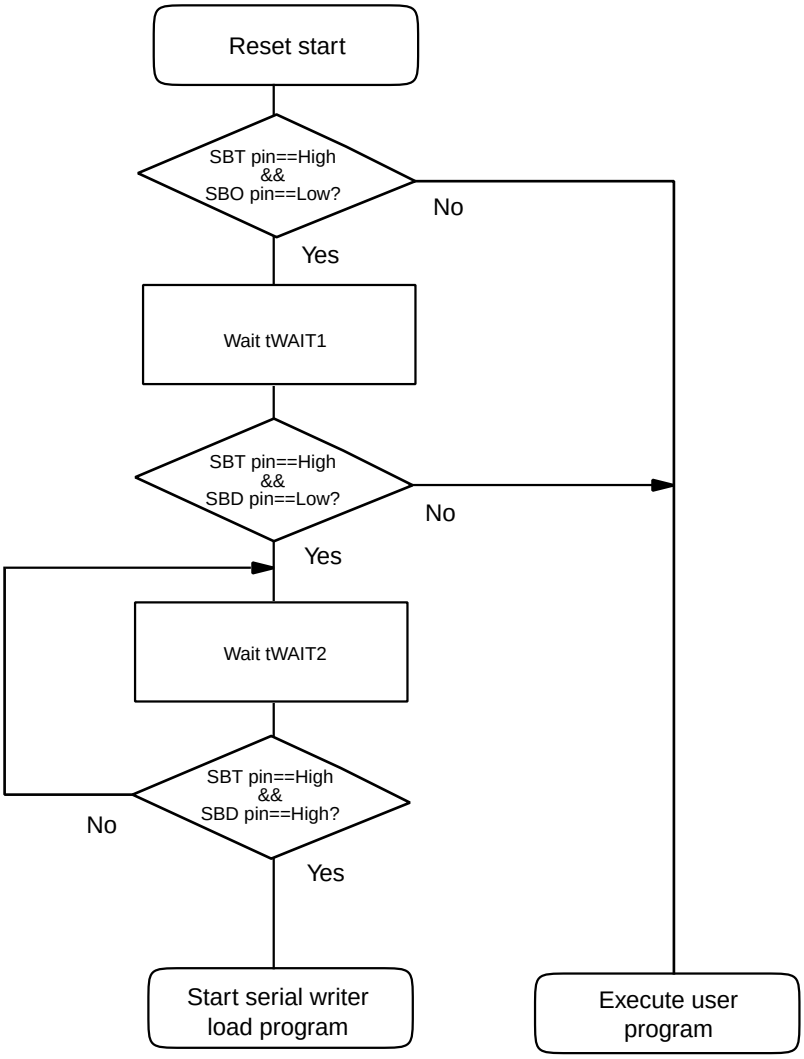


Figure 9-6-9 Start Routine for the Load Program

Conditions:

(1) After the load program initiates a reset start, SBD must be low and SBT high.

(2) Wait tWAIT1.

(3) SBD must be low and SBT high.

(4) Within tWAIT2, both SBD and SBT must be high.

If any of these conditions is not met, control returns to the user program.

9-6-9 Branching to the User Program

1. Branching to the reset start routine

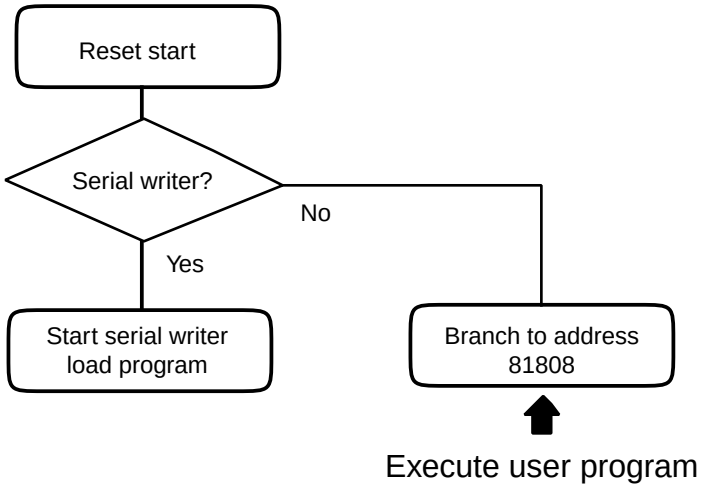


Figure 9-6-10 Branching to the reset start routine

When the reset starts, the serial writer load program initializes only if SBD is low. Otherwise, the program branches to the user program at address 0x81810.

2. Branching to the interrupt start routine

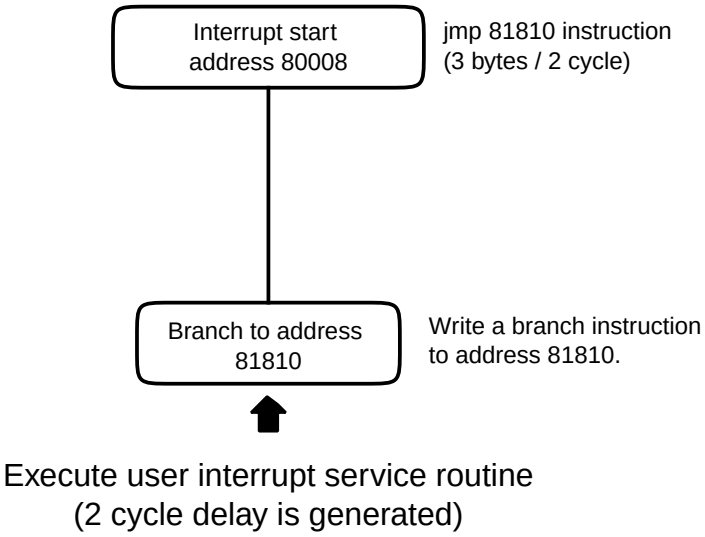

Interrupt start address 80008
jmp 81810 instruction (3 bytes / 2 cycle)
Branch to address 81810
Write a branch instruction to address 81810.
Execute user interrupt service routine (2 cycle delay is generated)

Figure 9-6-11 Branching to the interrupt start routine

In the interrupt start address, place a simple branch instruction pointing to address 0x81810.

9-6-10 Serial Interface for Onboard Programming

■ Features

[Fixed length serial interface]

· Character length : 8 bits
· Transfer bit : LSB first
· Source clock : External clock
· Maximum transfer rate : 5 Mbps (at 20 MHz oscillating)
· Error detection : Overrun error
· Buffer : Transmission / reception buffer, transfer single buffer / reception double buffer

■ Data timing

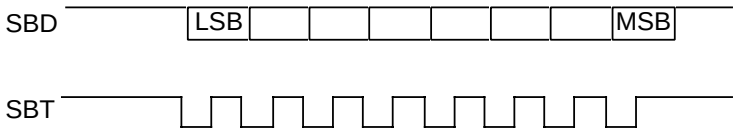


Figure 9-6-12 Data Transfer Timing

Serial data is transferred in 8 bits / LSB first.

■Register Configuration

Fixed length serial transmission/reception buffer

Register :SFTRB
Address :x'00FD72'
Use :Holding of serial transmission/reception data

Bit No.	7	6	5	4	3	2	1	0
Bit	SFT RB7	SFT RB6	SFT RB5	SFT RB4	SFT RB3	SFT RB2	SFT RB1	SFT RB0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
At reset	0	0	0	0	0	0	0	0
Read	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

bit	Description
7-0	Transmission/reception buffer 8 bits

Fixed length serial status register

Register :SFSTR
Address :x'00FD73'
Use :Display of serial transmission/reception status

Bit No.	7	6	5	4	3	2	1	0
Bit	SFT EN	SFR EN		SFB SY	SFT XA	SFR XA	SFT OE	SFR OE
Access	R/W	R/W	R	R	R	R	R	R
At reset	0	0	0	0	0	0	0	0
Read	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

bit	Description
0	With/without reception overrun error
1	With/without transmission overrun error
2	With/without reception data
3	With/without untransmission data
4	Transfer status flag transfer enable/ transfer in progress
5	Reserved
6	Reception disable/enable
7	Transmission disable/enable

9-6-11 PROM Writer / Onboard Serial Programming

■ Reprogramming flow

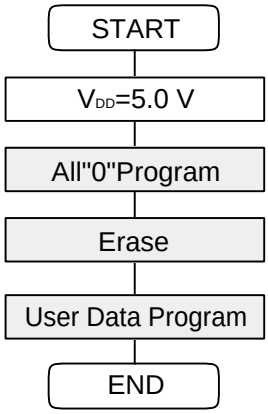


Figure 9-6-13 Reprogramming Flow

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